Design and Optimization of FPGA Power Solution with Power Modules

12/2018

杨恒

Outline

Part I. Introduction

- Background
- Challenges in FPGA power solution design

Part II. Optimum Design of FPGA Power Solution

- Power architecture of FPGA applications
- Typical requirement for FPGA power
- Advantage of power module solution
- Reference design with MPS power modules

Part III. Replacing the LDO with Power Module

- Limitation of single stage filter
- Two-stage filter design

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FPGA Applications

- CloudRAN
- Massive MIMO
- Backhaul
- Fronthaul
- Baseband
- Small Cell

5G Wireless

Embedded Vision

- ADAS
- Machine Vision
- 8K Display & Transport
- Surveillance
- Military Vision Systems
- Drones

- Motion Control
- Machine-to-Machine
- Preventative Maintenance
- Smart Energy and Grid
- Smart Medical
- Big Data Analytics

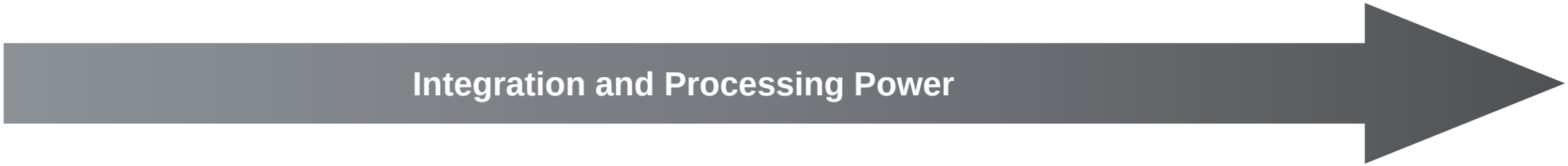
Industrial IoT

Cloud Computing

- CloudRAN
- Deep Neural Networks
- Image and Speech Recognition
- Video in the Cloud
- Big Data Analytics
- Data Center Interconnect
- SSD Storage

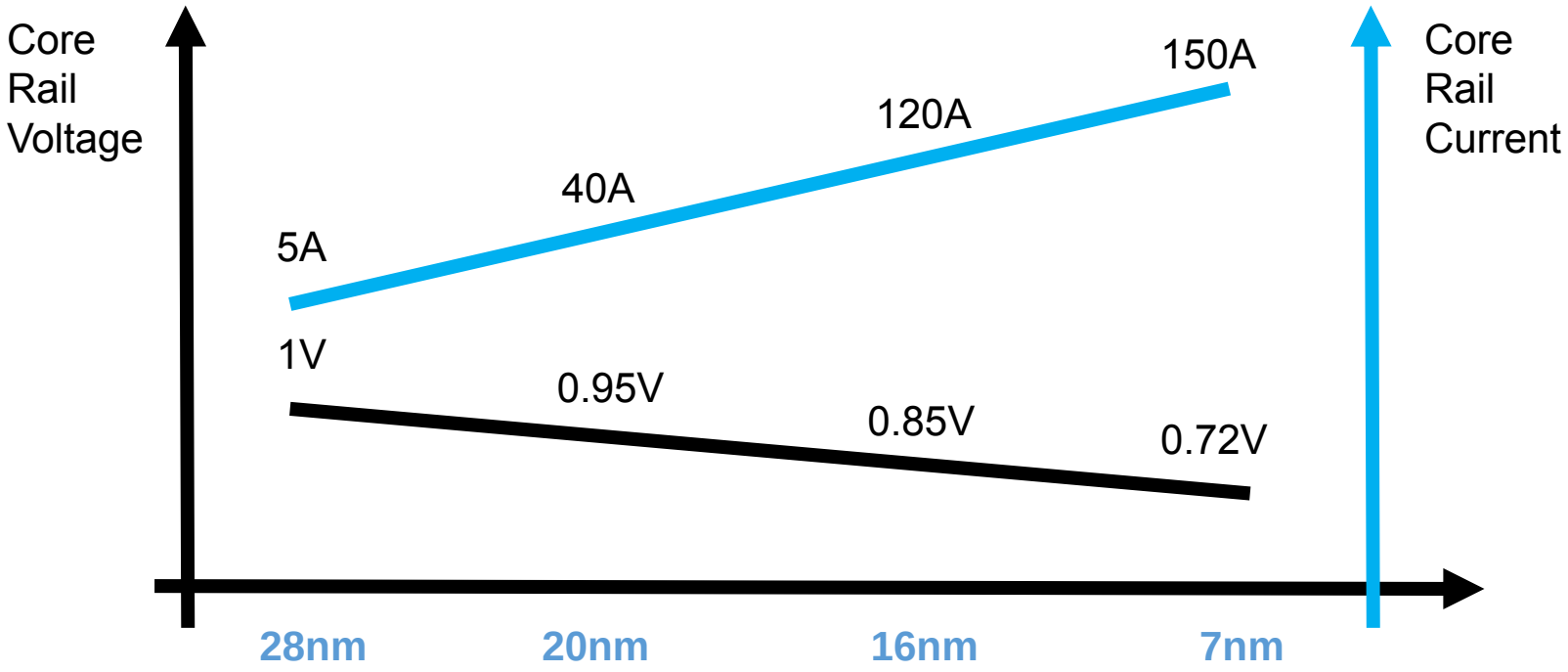
Finer Process Demands for Higher Power

28nm	20nm	14nm
Arria® V Stratix® V	Intel® Arria® 10	Intel® Stratix® 10



28nm	20nm	16nm	7nm
VIRTEX 7 KINTEX 7 ARTIX 7 SPARTAN 7	VIRTEX UltraSCALE KINTEX UltraSCALE	VIRTEX UltraSCALE+ KINTEX UltraSCALE+	XILINX VERSAL™

Lower Core Rail Voltage and Higher Current

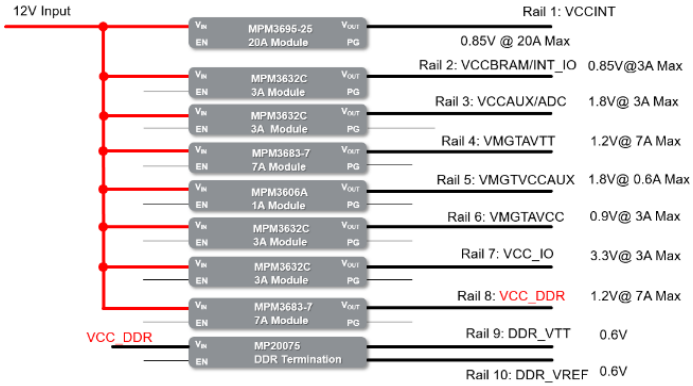


Power Modules Address FPGA Power Design Challenges

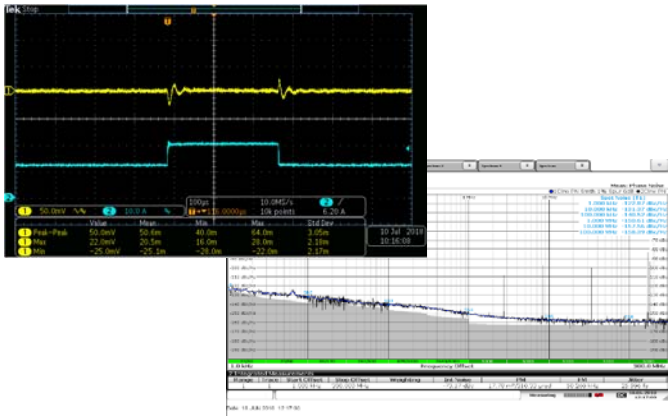
Example:

Xilinx 7nm Versal ACAP

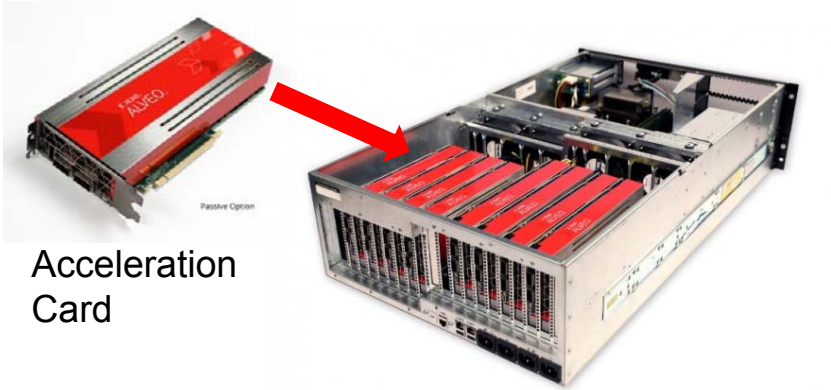
Complex Rail Combination



<3% Accuracy & Low Noise

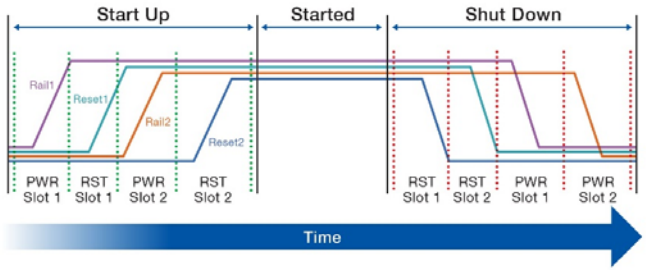


Limited Space & Height



Acceleration Card

Power Up & Down Sequence



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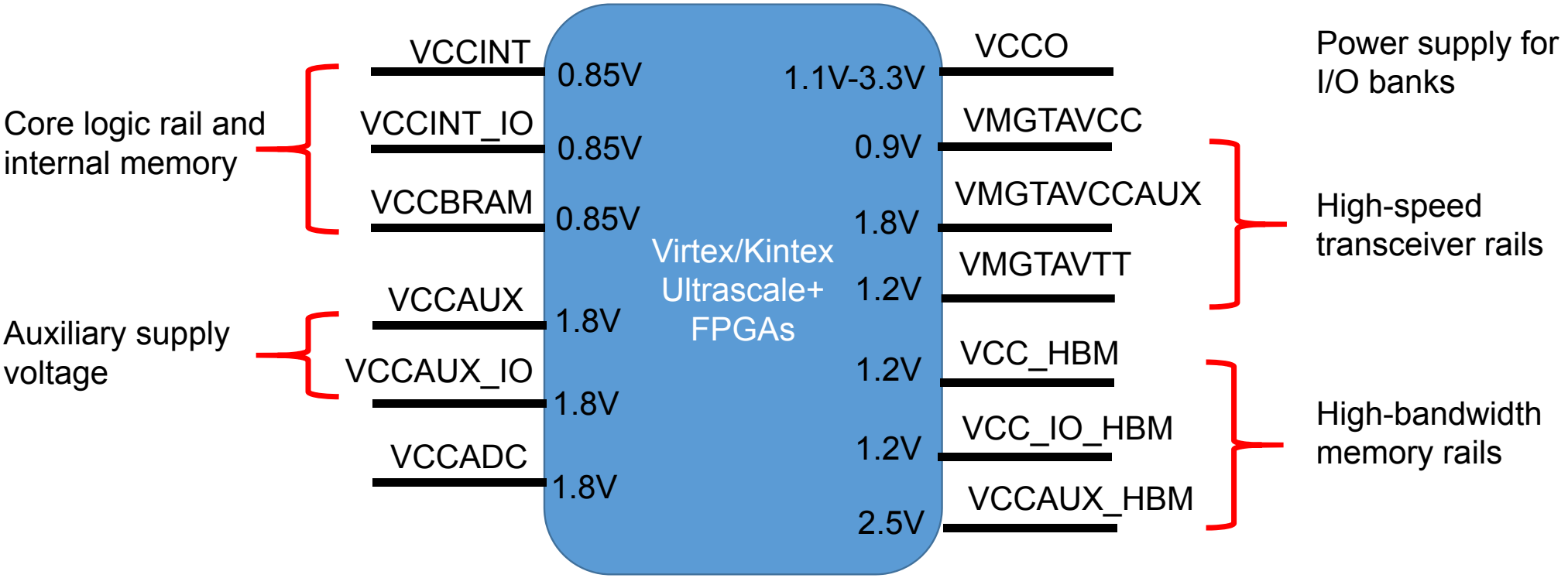
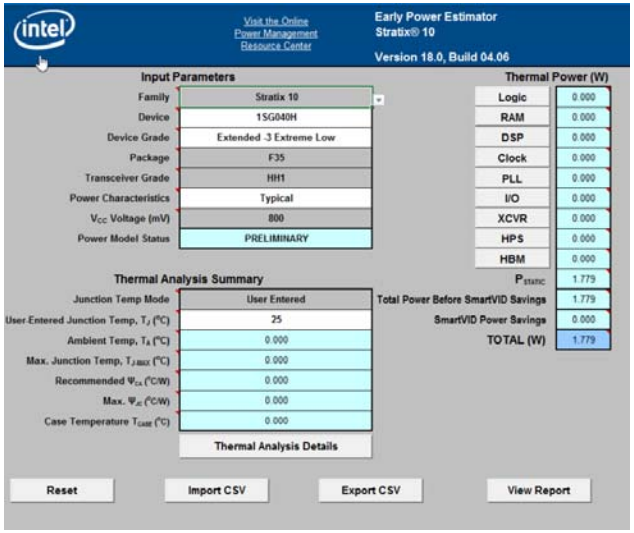
Typical Architecture FPGA Power Solution

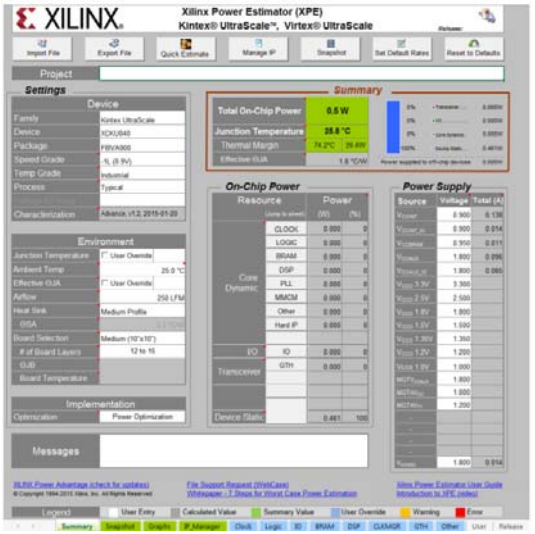


Leverage Power Design Tool's from FPGA Vendors

Power/current estimation based on specific application



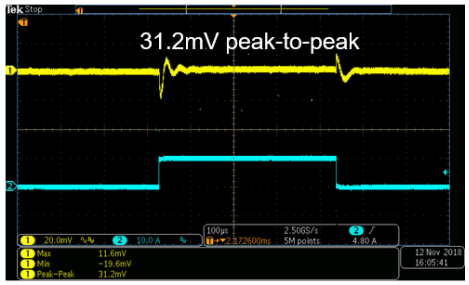
- Altera Early Power Estimation Tool



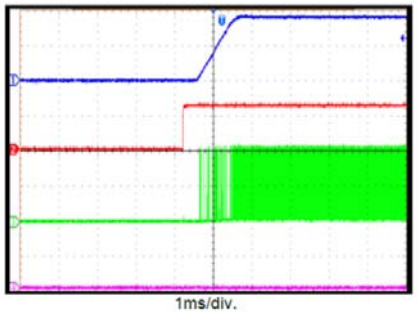
- Xilinx XPE Tool

Typical Power Requirement for FPGAs

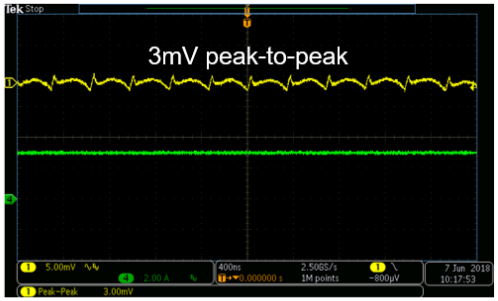
Maximum deviation during core rail load transient



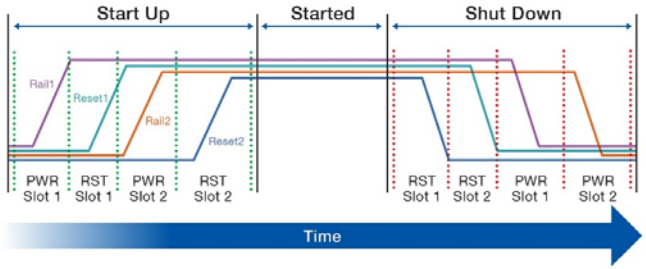
Monotonic start-up



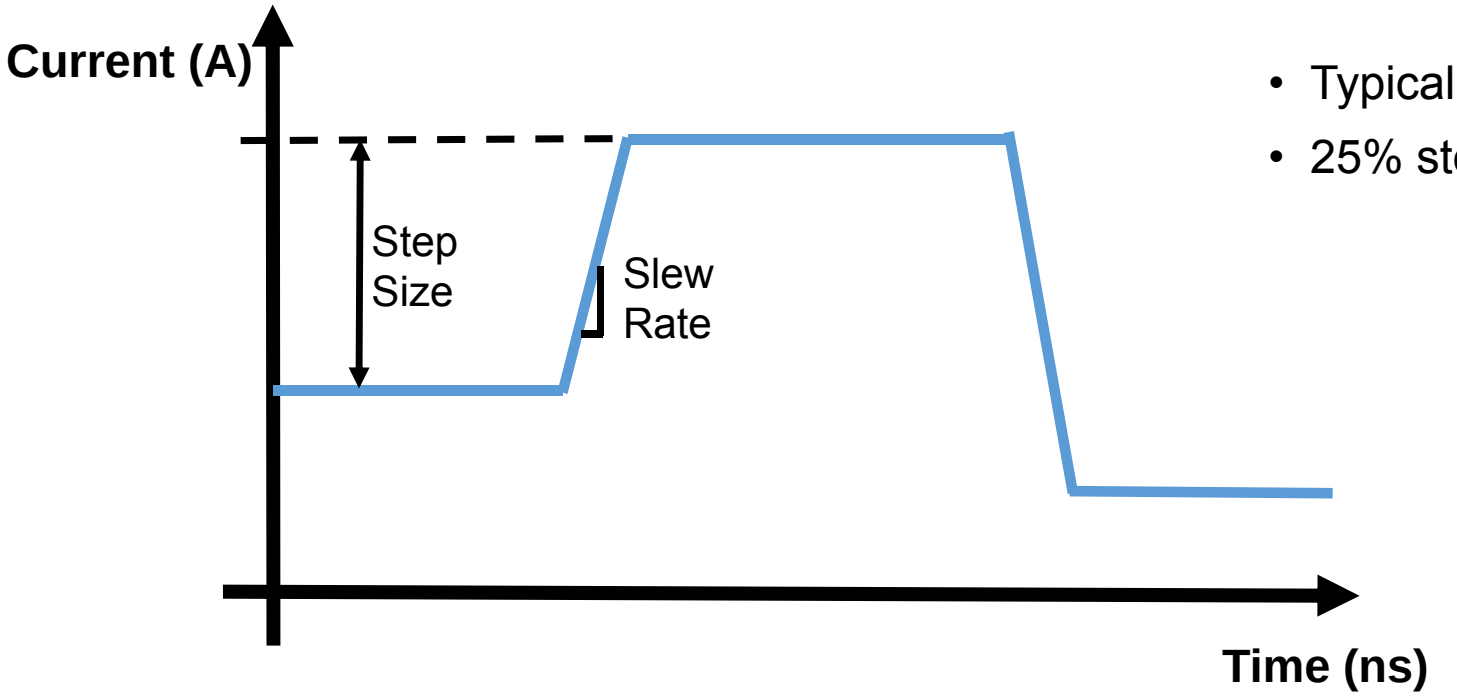
Maximum peak-to-peak ripple for sensitive rails



Sequence requirement

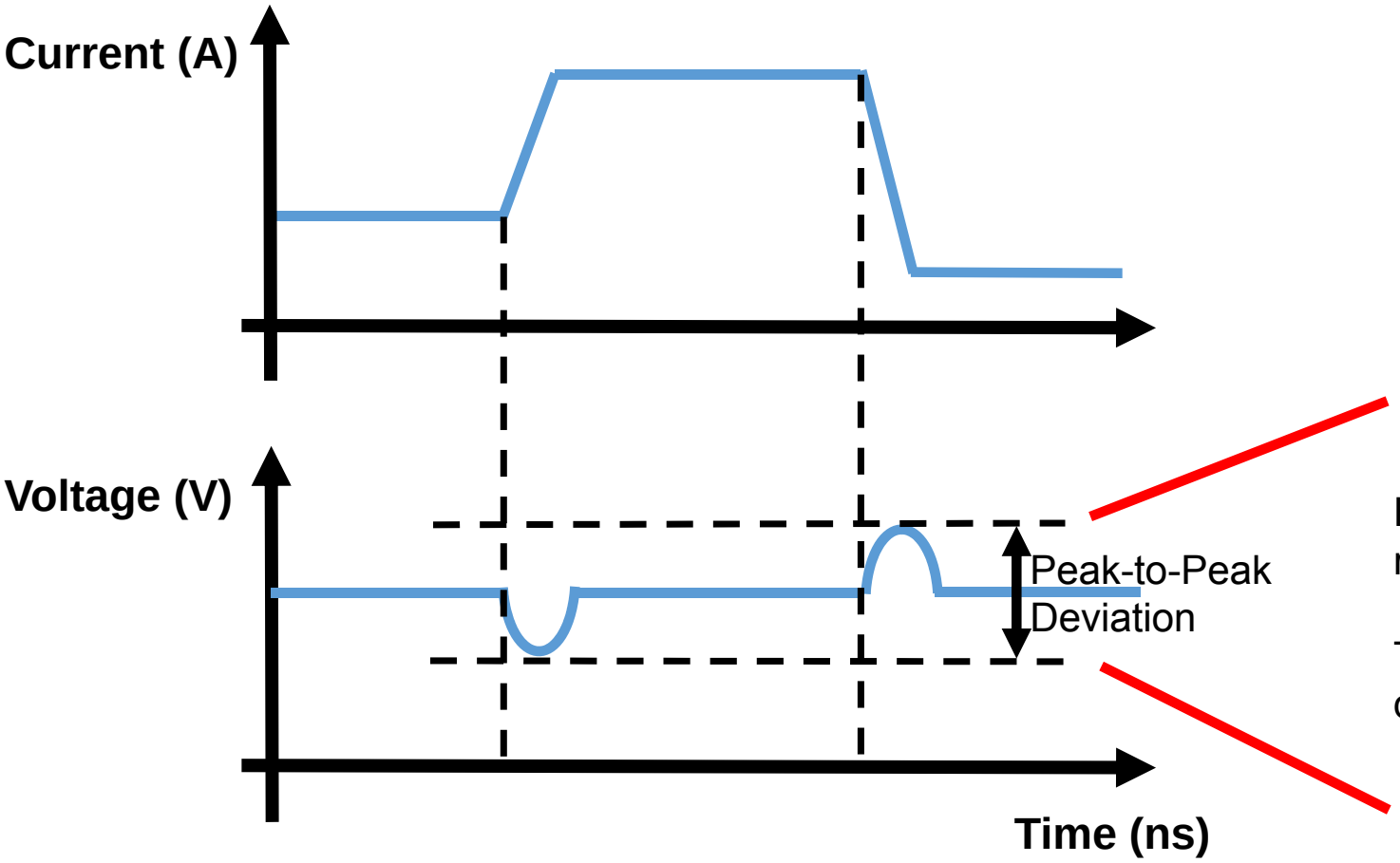


High-speed Transient Required by FPGA Core



- Typical Xilinx Specification
- 25% step size at 100A/us

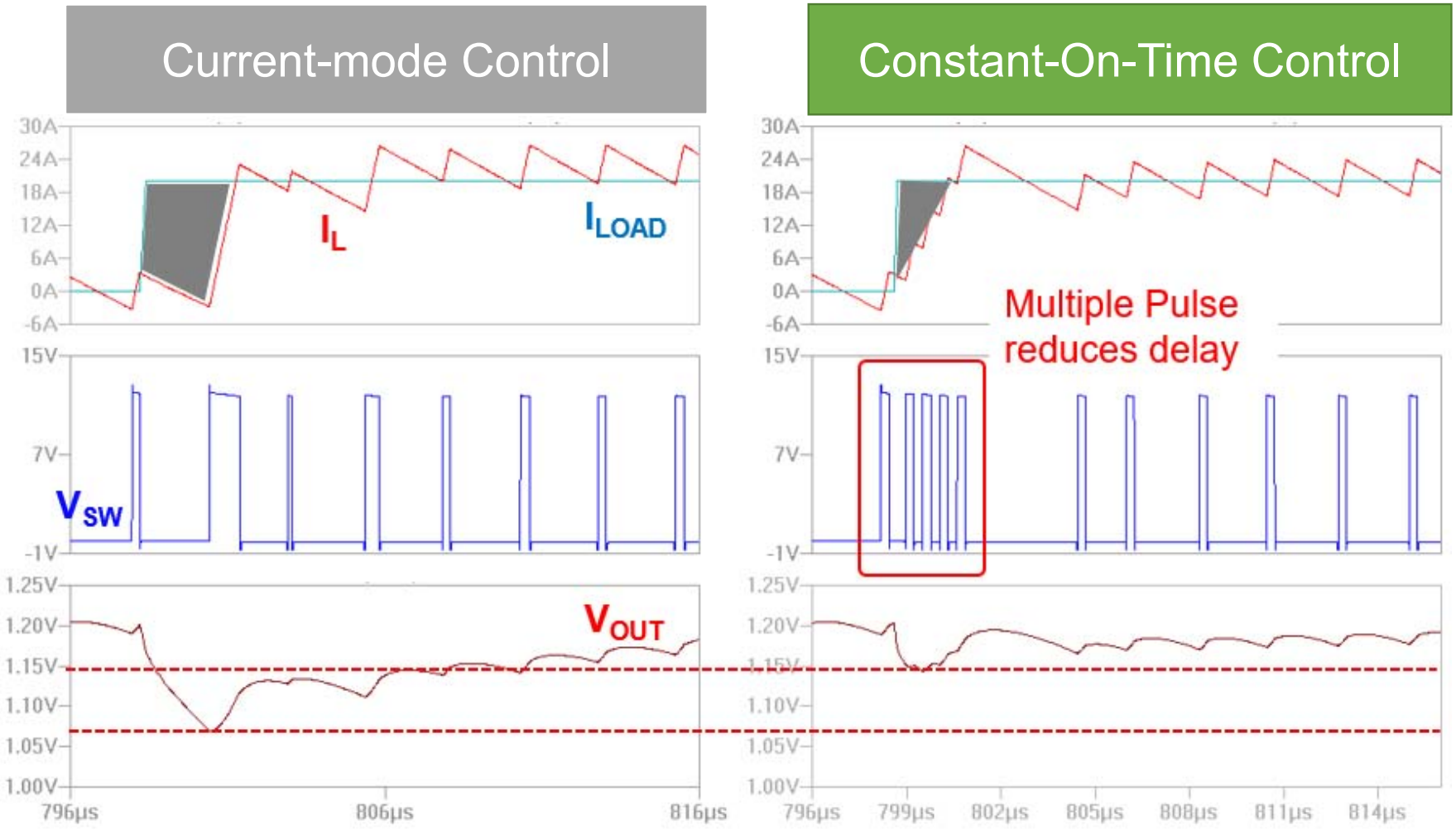
High-speed Transient Required by FPGA Core



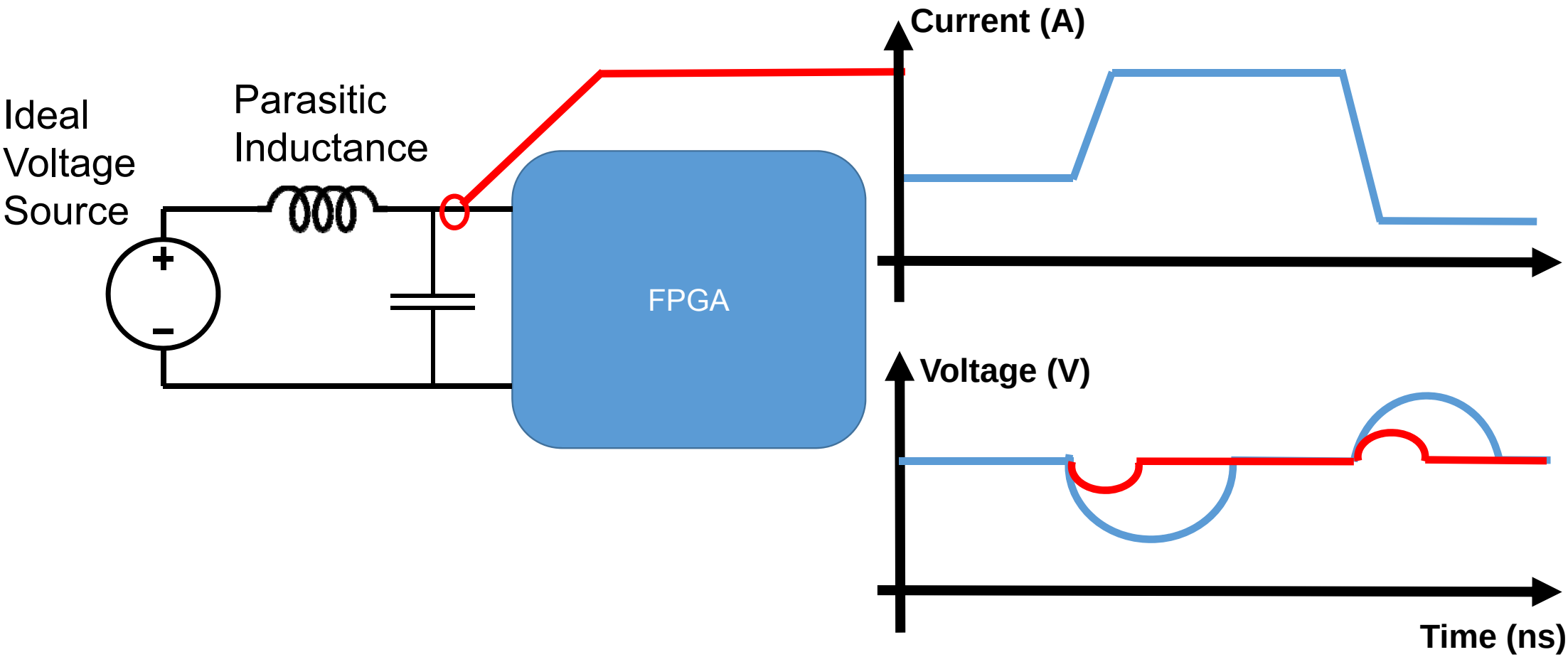
How fast the control loop response to a voltage drop

The design and quality of decoupling/bypass capacitors

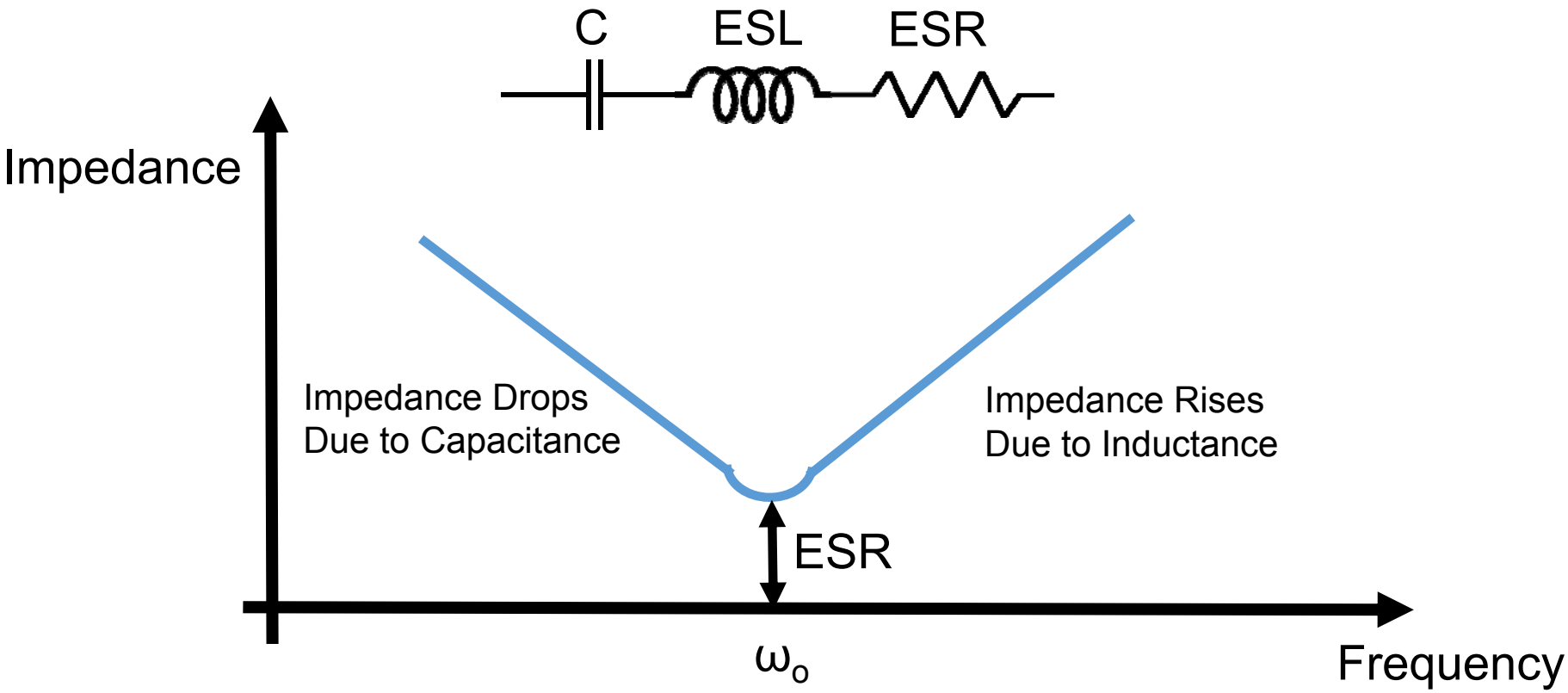
Use COT Control to Achieve Faster Transient Response



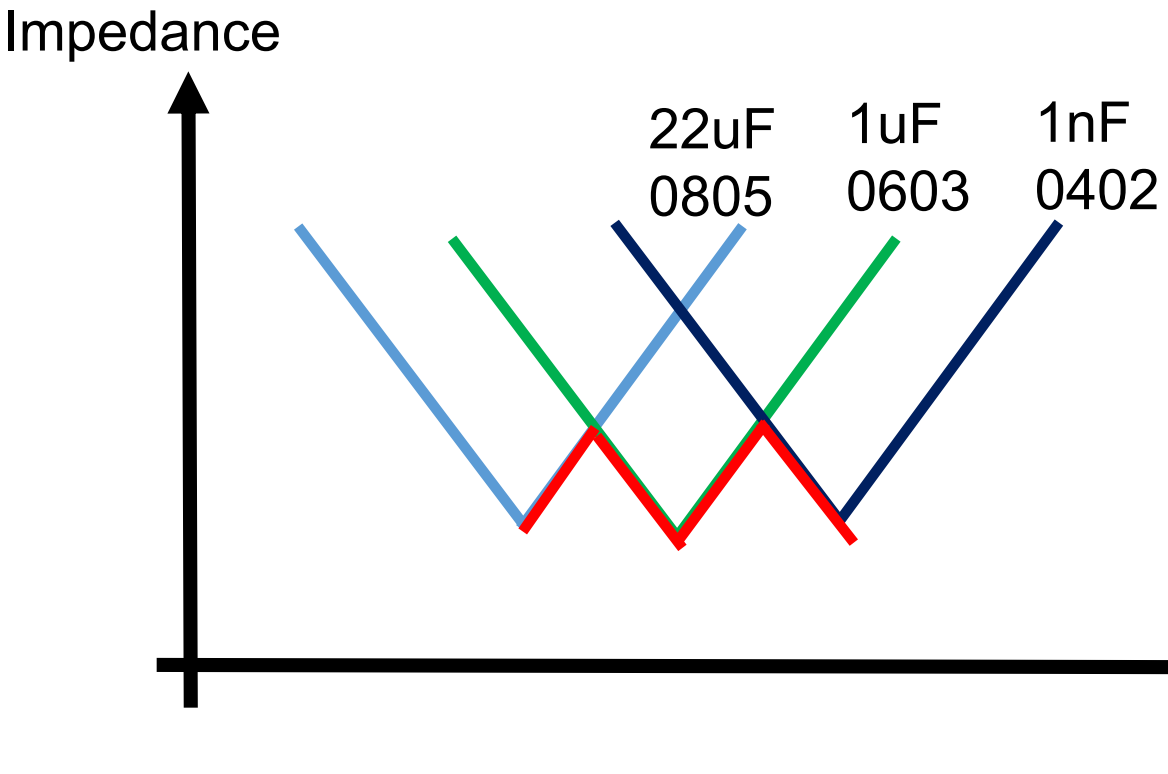
Why Do I Need Bypass/Decoupling Capacitors?



Non-ideal Decoupling Capacitor

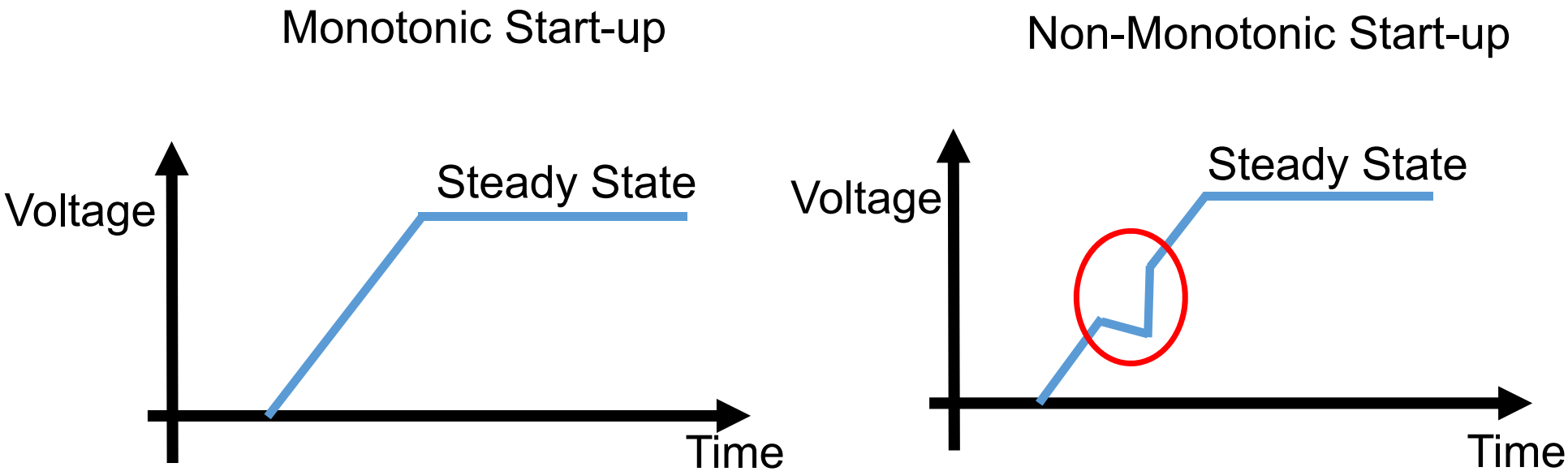


Decoupling Capacitors



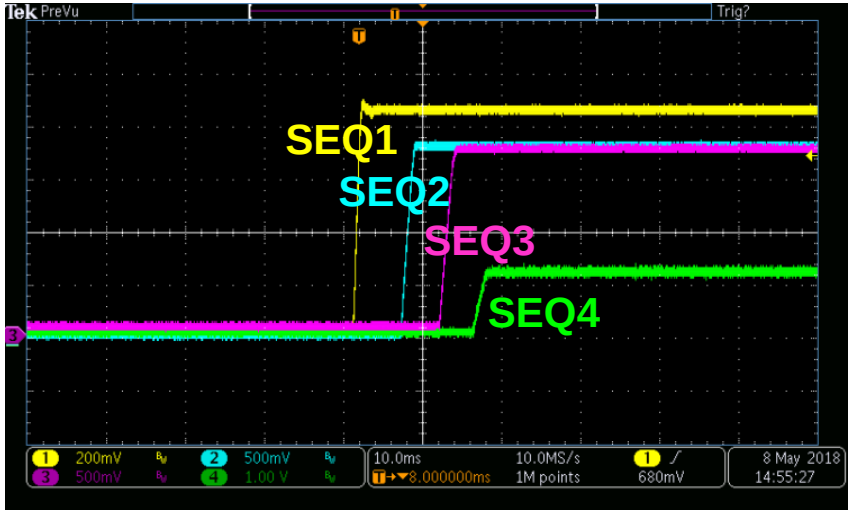
- Use a combination of different type and values of capacitors
- Place the small package capacitor on the bottom of FPGA
- Use SP-Cap to provide bulk capacitance

Monotonic Start-up

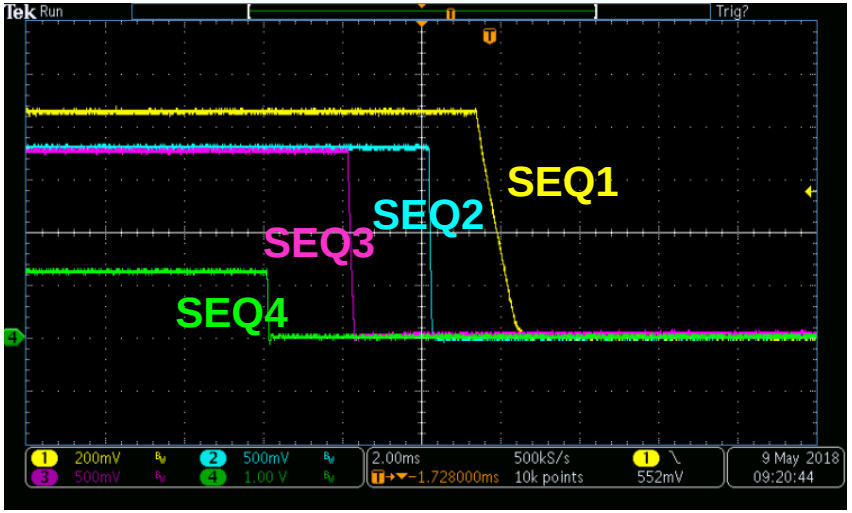


Sequence Requirement

Start-up Sequence

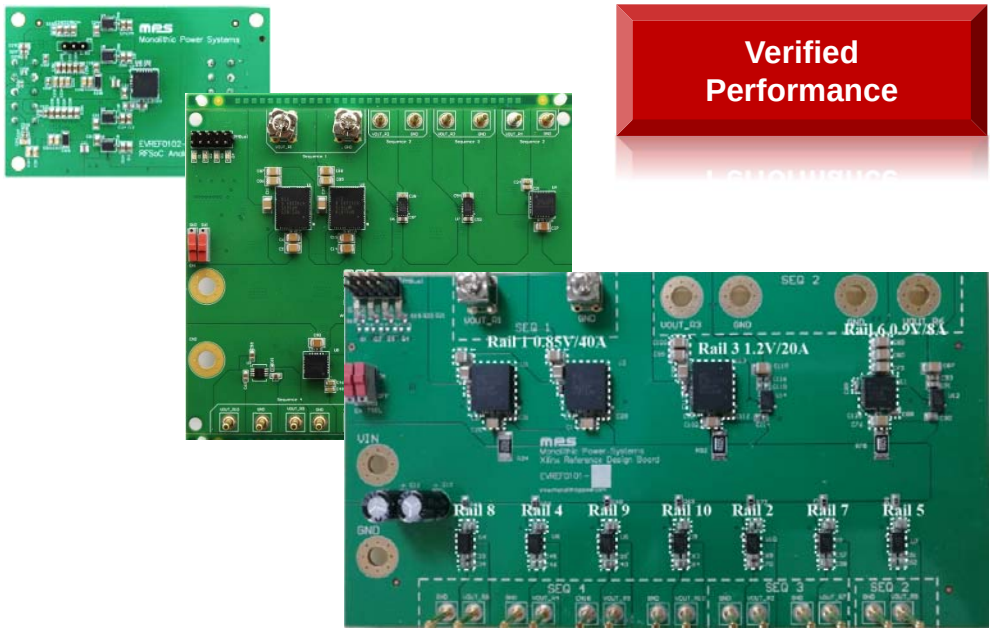


Shut-down Sequence



- Recommended:
  - o Use sequencer chip to control the start-up and shut-down sequences
  - o Use built-in sequencing control – MPM54304
- Not recommended:
  - o Connect PG and EN in an cascaded manner

Advantages of Power Module Solution



Verified Performance

Fully integrated power module solution

Rich Design Resource Online

- FPGA Reference design package
- EVB Design Files (SCH, Layout…)
- MPSmart Simulation Model
- Module Layout Component Library
  - Allegro & Altium
- 3D STEP Model
- Application notes/Articles
- Reliability Report

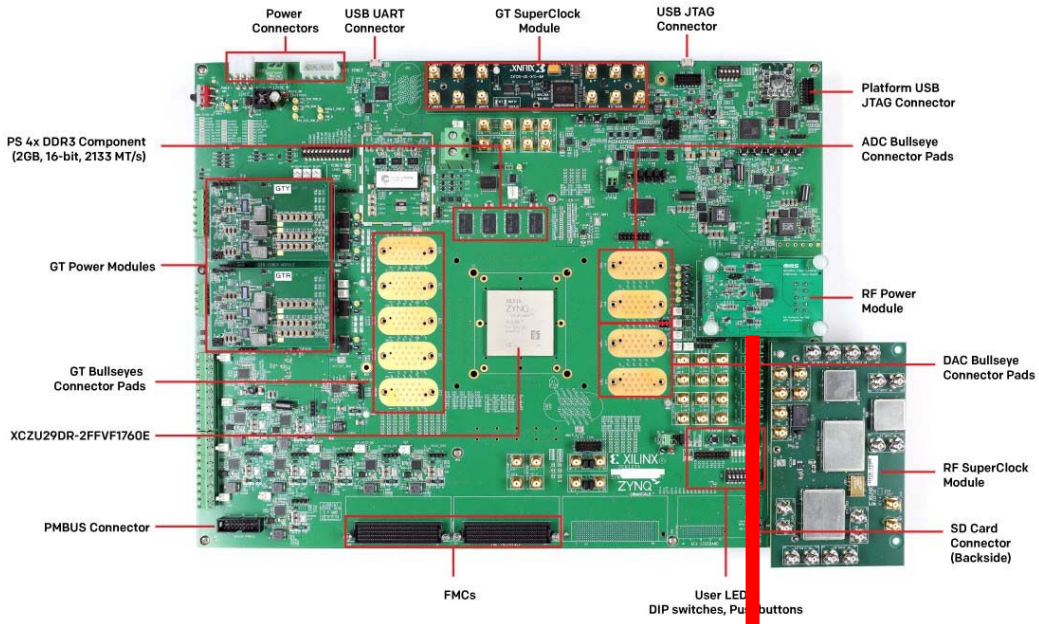
https://www.xilinx.com/products/technology/power.html#partners
https://www.monolithicpower.com/en/design-tools/reference-design-partners/xilinx-reference-design.html

Partnership with Xilinx

MPS is partnered with Xilinx on power reference designs

- Xilinx Zynq US+ RFSoc Development kit
- Spartan-7 reference design board with full MPS power solution
- More activities are coming!

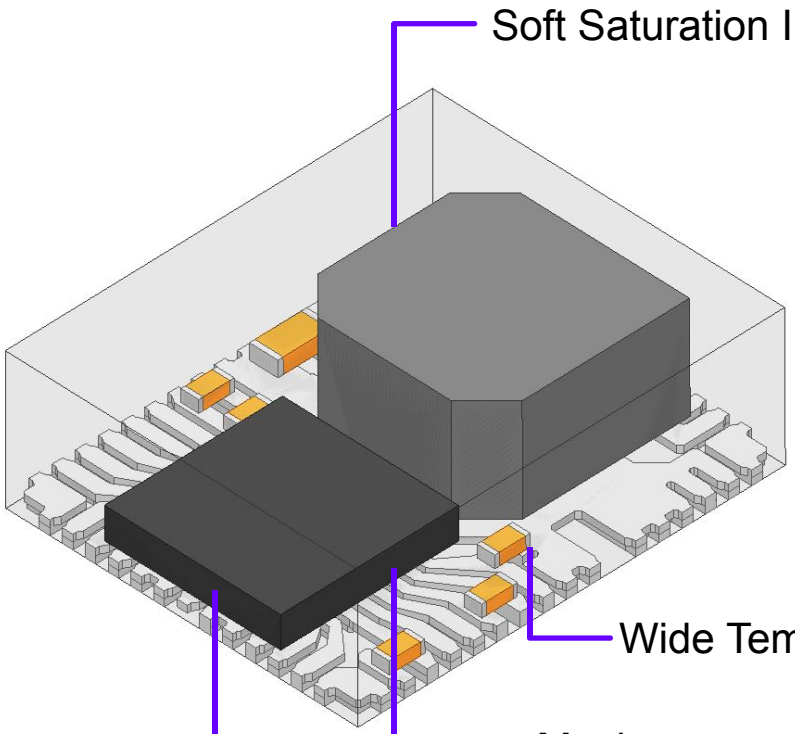
Xilinx Zynq US+ RFSoC ZCU1275 Development kit



MPS EVREF0102 Power Module

- Full module solution
- Power RF 12-bit 2GSPS ADCs and 14-bit 6.4GSPS DACs rails
- Ultra-low noise - <1mV Ripple

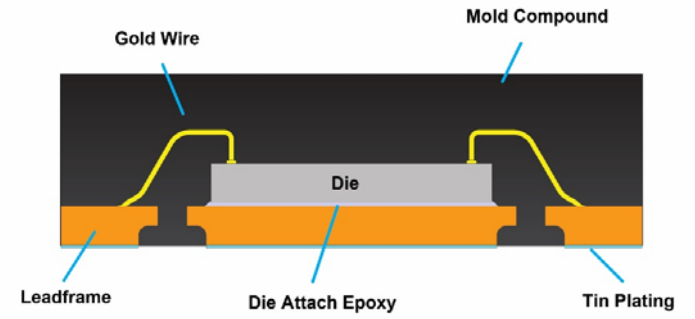
Advantages of MPS Power Modules



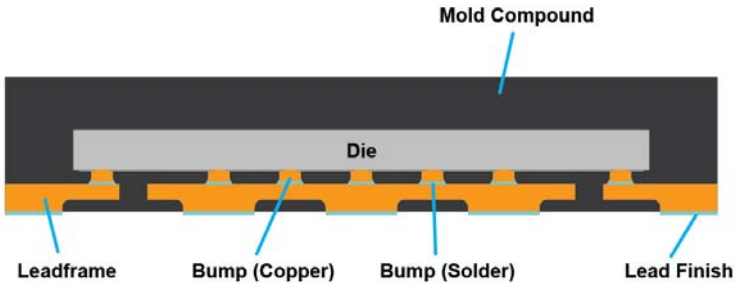
- **Small-size**
- **High-efficiency**
- **Ease of Use**
- **Short Time-to-market**

MPS Advanced Packaging Technology

Wire Bond



Mesh Connect™
(No Wire Bond)



High Reliability, Small Form Factor, Better Heat Dissipation, Minimized Inductance, and Faster Response

Product Selection Guide for FPGA Power

Step 1 → **Check Voltage Rail Requirement**

Step 2 → **Estimate Rail Current**

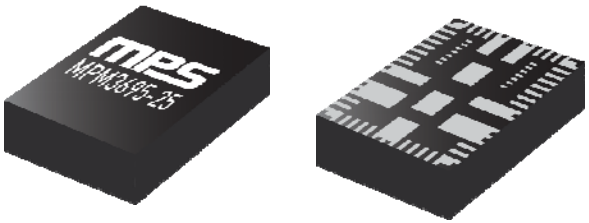
Step 3 → **Select MPS Power Module Product**

Step 4 → **Get Support if Optimization needed**

	10mA-300mA	300mA-1A	1A-3A	3A-4A	4A-8A	8A-20A	20-40A
12V Input	MPM3606A	MPM3606A	MPM3632C	MPM3683-7	MPM3683-7	MPM3695-25	2xMPM3695-25
5V Iniput	MPM3805	MPM3811	MPM3833C	MPM3840	MPM3683-7	MPM3695-25	2xMPM3695-25
DDR Termination	MP20075						

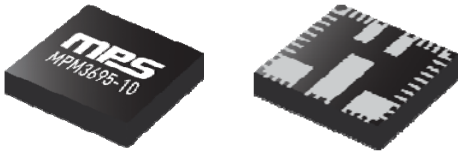
Intelligent Scalable DC-DC Power Module Family

MPM3695-25



- 16V, 20A power module with integrated inductor
- Scalable for higher current
- 10mm x 12mm x 4mm LGA package

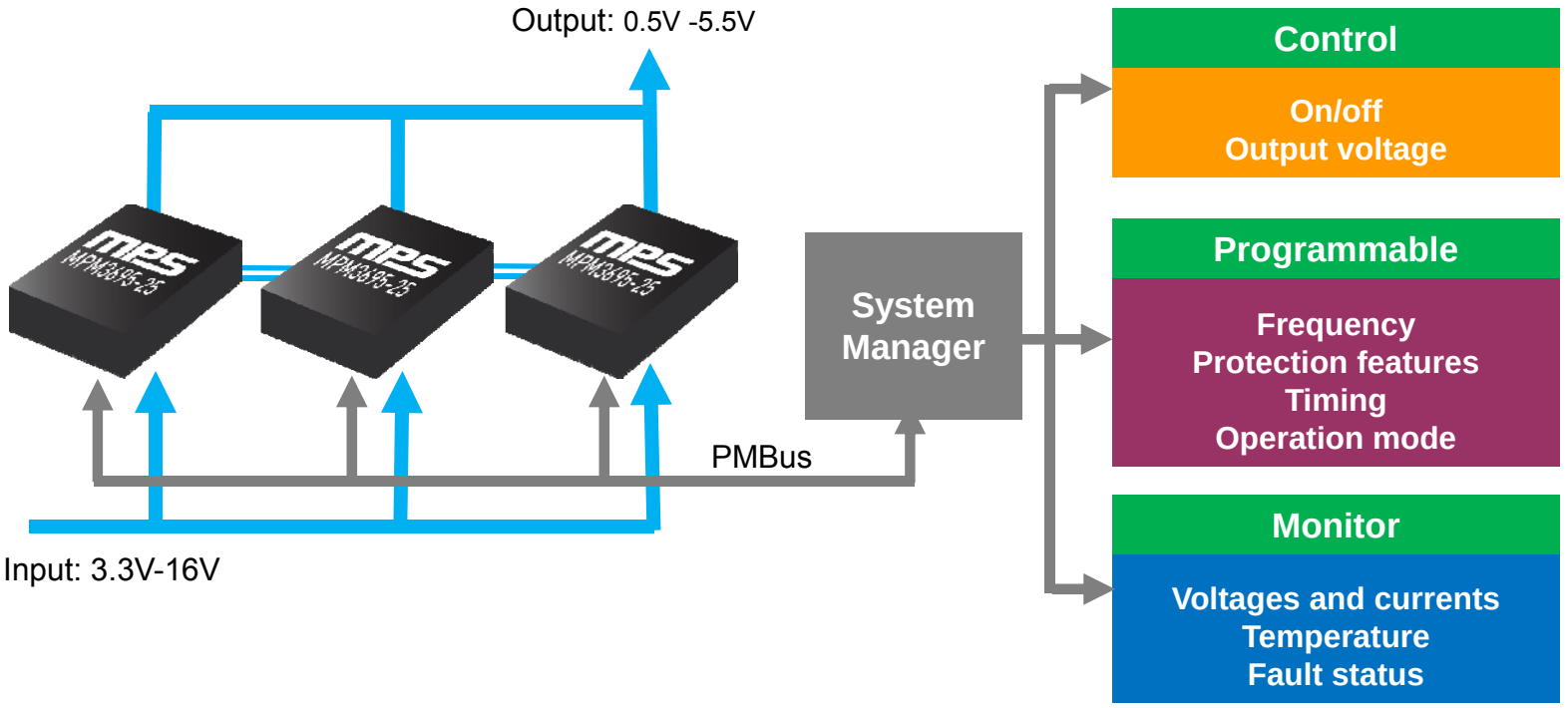
MPM3695-10
MPM3695A-10



- 14V, 7A/10A power module with integrated inductor
- Scalable for higher current
- 8mm x 8mm x 1.6mm ultra-thin LGA package

- No compensation network required
- Differential Remote Voltage Sensing
- Programmable via PMBus:
  Current Limit, SS, FSW, OCP, UVP, OVP, OTP limit
- Versatile solution to FPGA and ASIC core power

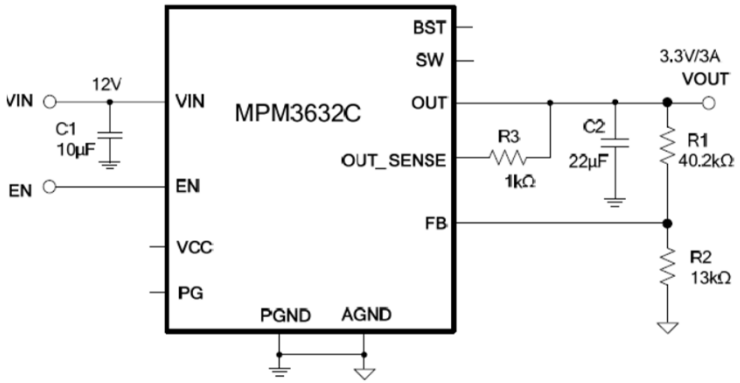
Intelligent Scalable DC-DC Power Module Family



MPM3632C (18V, 3A, Low Voltage Ripple)

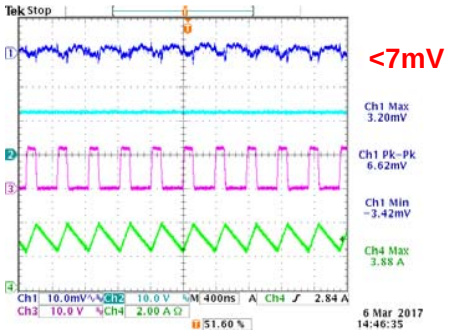
FEATURES

- 4V to 18V Input voltage range
- 3A continuous current
- 0.8V to 5.5V output voltage range
- 0.5% accuracy of V_{FB}
- Fixed 3MHz Fsw
- Force CCM operation
- Power-good pin
- OCP/OTP/UVLO protection features



Available in a QFN (3mmx5mmx1.6mm) Package

$12V_{IN}$, $1.8V_{OUT}$
C_{OUT}=1x22uF



<7mV

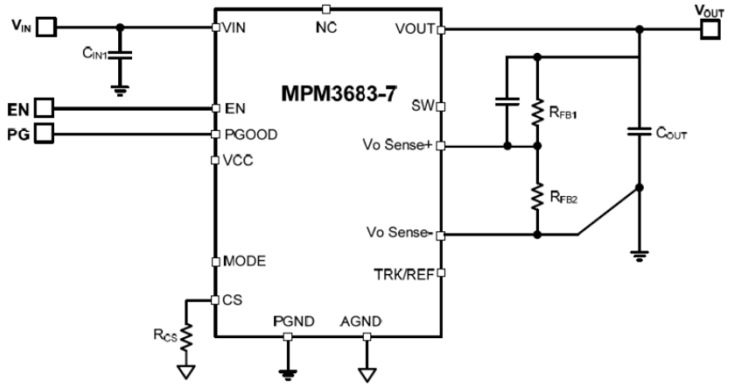
Applications

- FPGA/ASIC POL converters
- Networking/servers
- LDO replacement
- Space constraint applications

MPM3683-7 (16V, 8A Module)

FEATURES

- Wide 4V to 16V input range
  - 2.7V to 16V with external 3.3V VCC
- Output voltage range: 0.6V to 5.5V
- Continuous 8A / peak 10A output current
- Differential output voltage remote sense
- Output voltage tracking
- Power-good indication
- ±1% maximum output regulation error in the range of -40~125℃
- Adjustable switching frequency
- Selectable PFM or Force CCM mode
- Non-Latched OVP/UVP/OCP/OTP protection features
- Available in QFN-32, 7mm x 7mm x 4mm

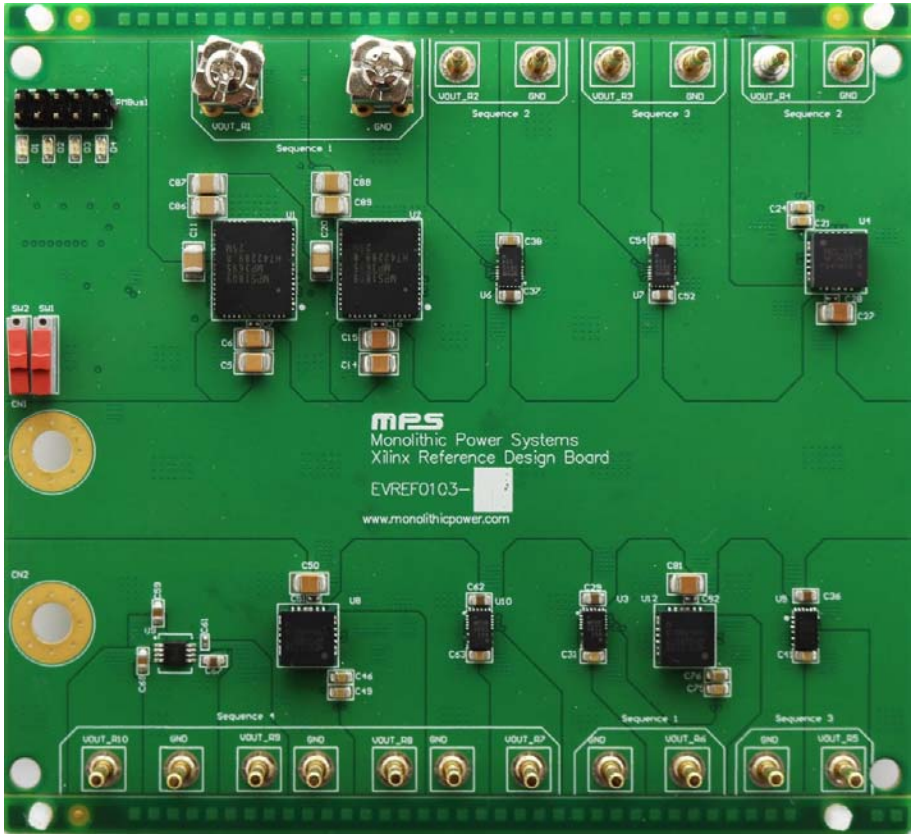


Available Reference Designs for Xilinx FPGAs

FPGA Series	FPGA Part Numbers	EVB #	# of Rails	Core Current
Kintex Ultrascale and Ultrascale+	KU13P, KU15P	EVREF0103-A	8	50A Max
	KU3P, KU5P, KU9P, KU11P	EVREF0103-B	8	25A Max
Zynq Ultrascale+ MPSoC	ZU9CG, ZU9EG, ZU11EG-ZU19EG	EVREF0101-A	13	50A Max
	ZU3CG to ZU7EV	EVREF0101-B	13	25A Max
Zynq 7000	XC7Z007S to XC7Z020, XC7Z030	EVREF0100-A	7	3A Max
Zynq Ultrascale+ RFSoC Analog Rails	ZU21DR to ZU29DR	EVREF0102-A	5	N/A

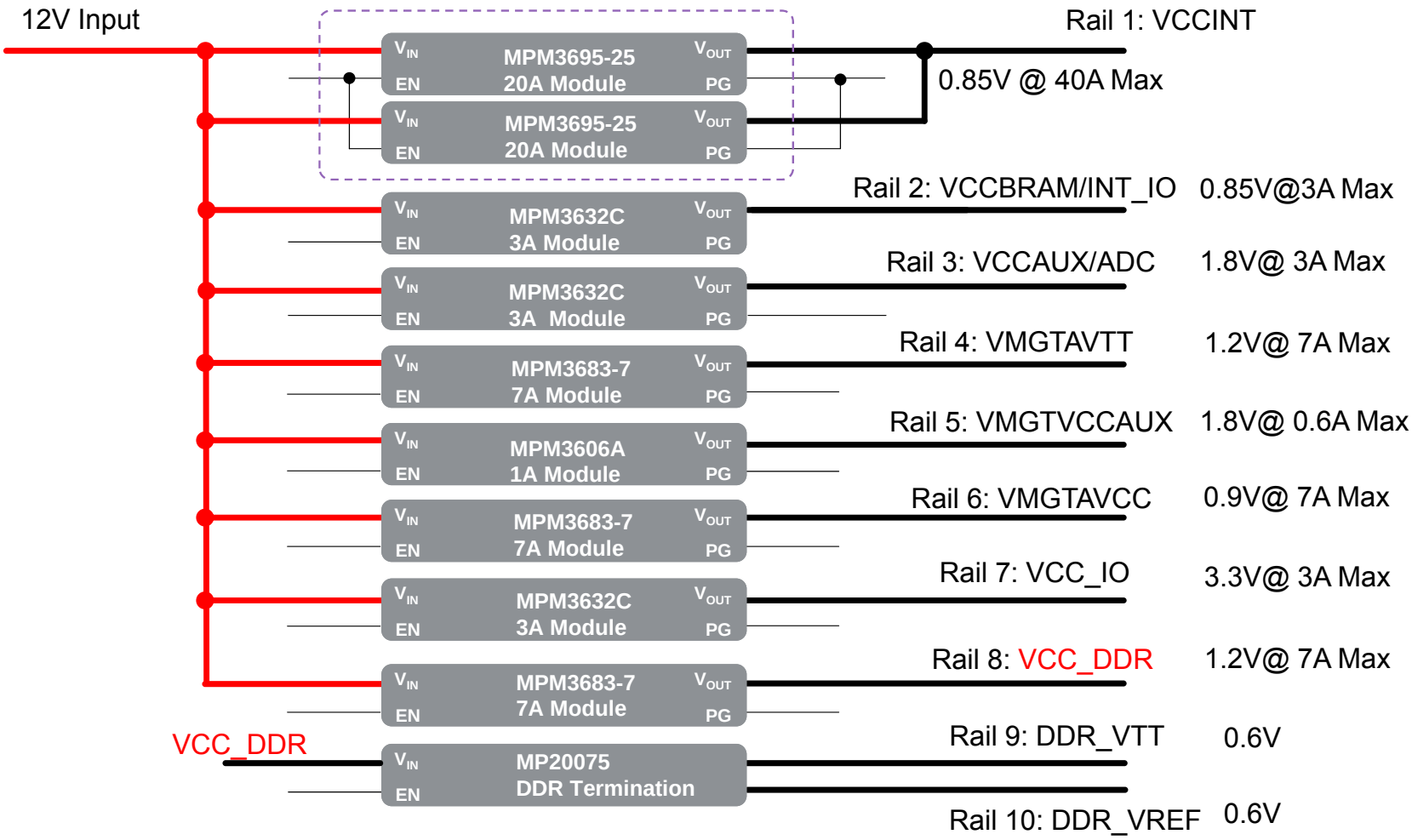
Complete Reference Design Available at:
https://www.xilinx.com/products/technology/power.html#partners and
https://www.monolithicpower.com/en/design-tools/reference-design-partners/xilinx-reference-design.html

Kintex Ultrascale+ Reference Design Board



FPGA Series	FPGA P/N	Demo Board P/N	Core Current
Kintex Ultrascale+	KU13P, KU15P	EVREF0103-A	50A Peak
	KU3P, KU5P, KU9P, KU11P	EVREF0103-B	25A Peak

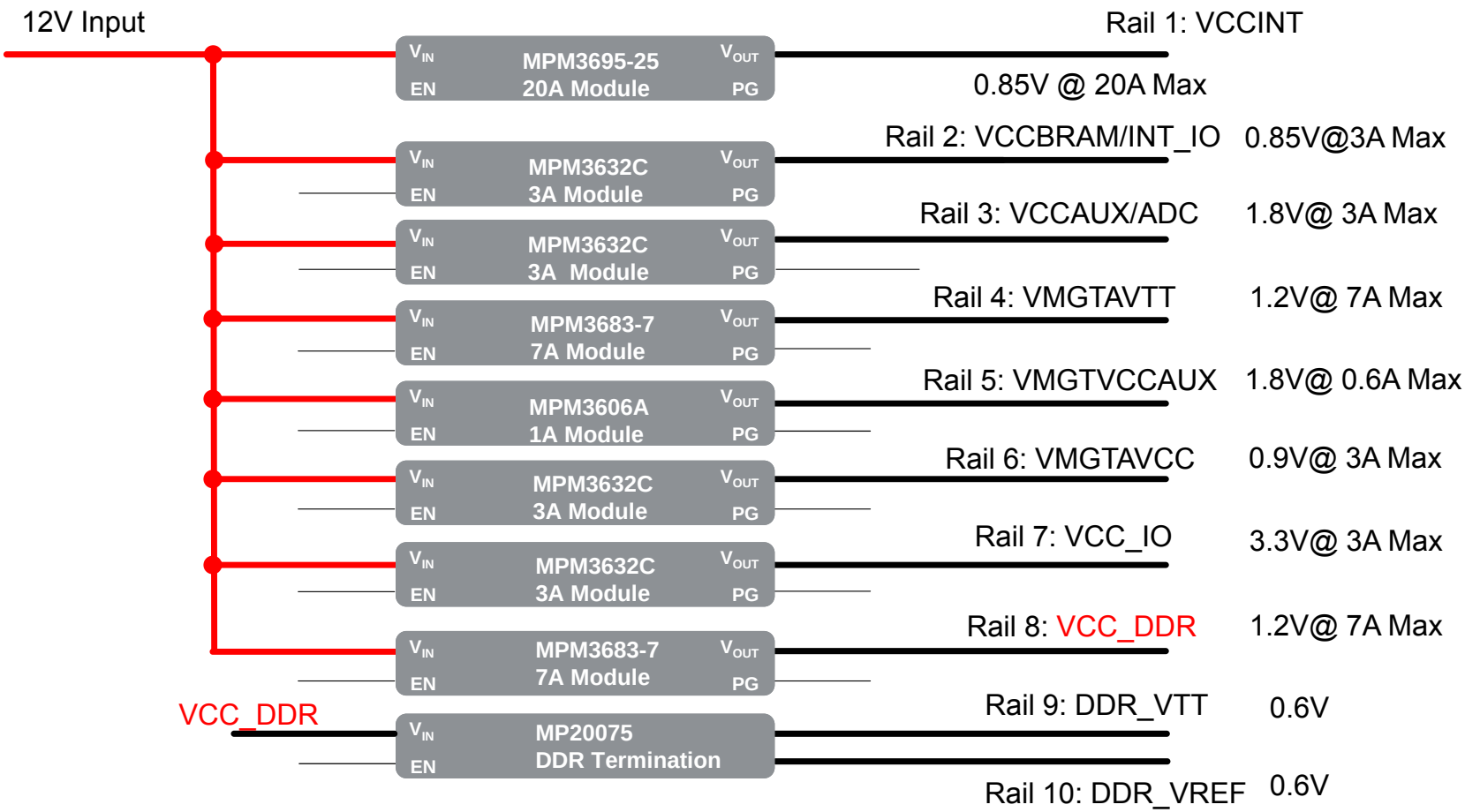
Solution Power Tree – High Power Version



Summary of High Power Version

Rail Number	Rail Name	VOUT	Limit	Max DC Load	Seq Up	MPS Part#
1	VCCINT	0.85V	±3%	40A	1	MPM3695-25 x2
2	VCCBRAM/ VCCINT_IO	0.9V	±3%	3A	2	MPM3632C
3	VCCAUX/ADC	1.8V	±3%	3A	3	MPM3632C
4	VMGTAVTT	1.2V	±3%	7A	2	MPM3683-7
5	VMGTVCCAUX	1.8V	±3%	0.6A	3	MPM3606A
6	VMGTAVCC	0.9V	±3%	7A	1	MPM3683-7
7	VCC_IO	3.3V	±3%	3A	4	MPM3632C
8	VCC_DDR	1.2V	±3%	7A	4	MPM3683-7
9	DDR_VTT	VCC_DDR/2	±3%	N/A	4	MP20075
10	DDR_VREF	VCC_DDR/2				

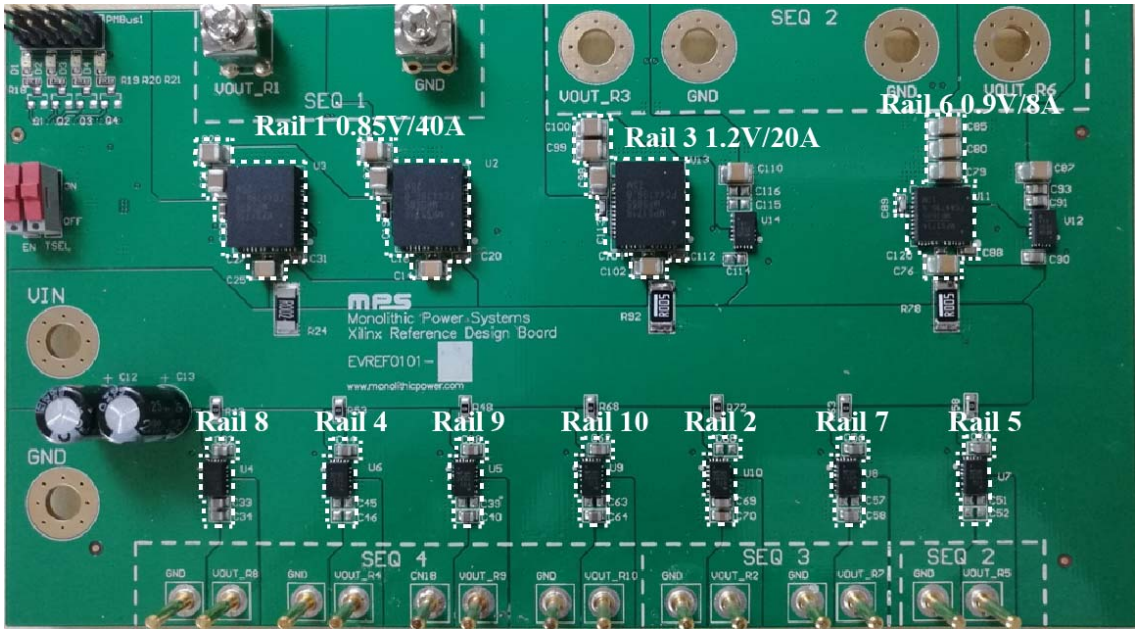
Solution Power Tree – Low Power Version



Summary of Low Power Version

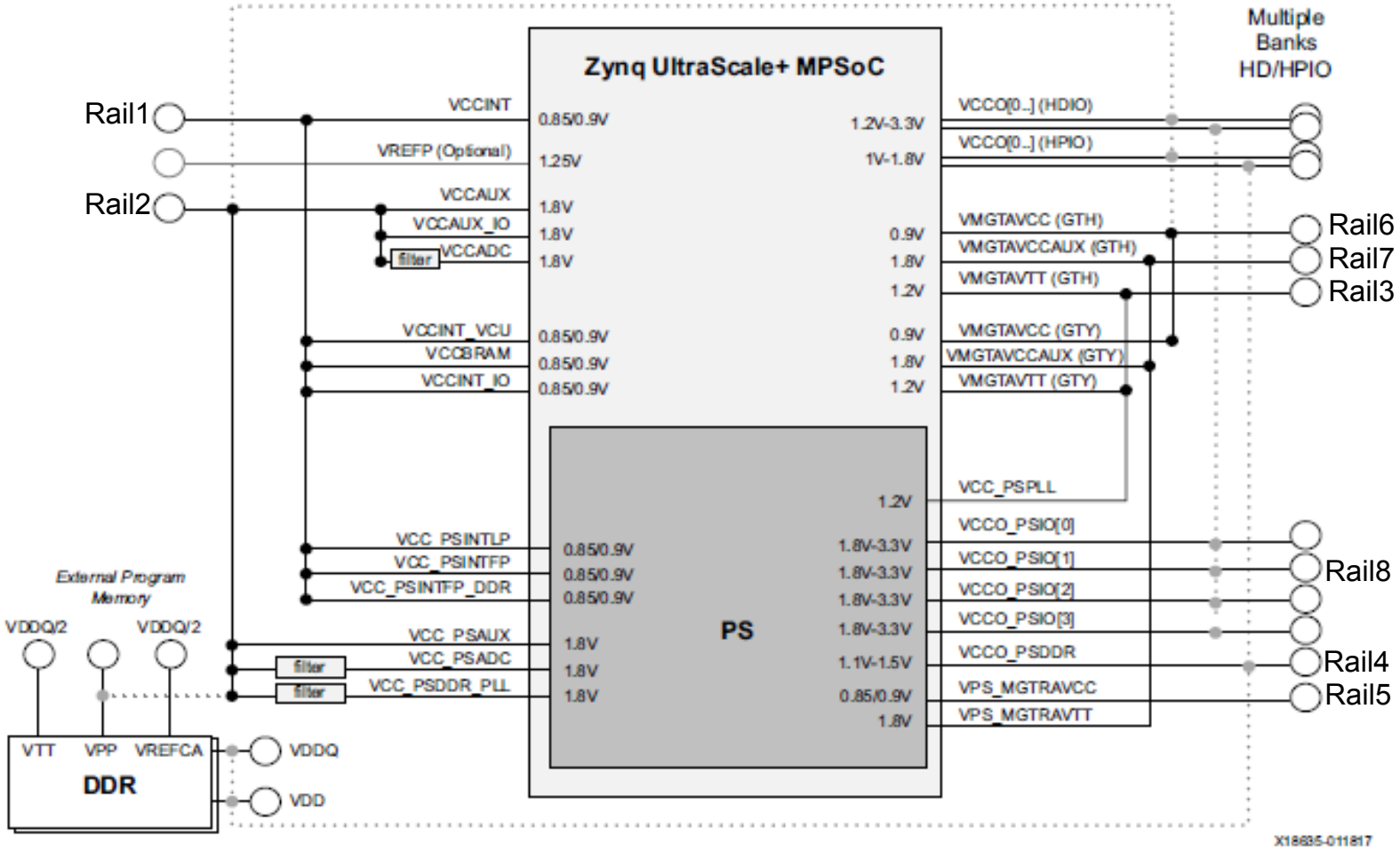
Rail Number	Rail Name	VOUT	Limit	Max DC Load	Seq Up	MPS Part#
1	VCCINT	0.85V	±3%	20A	1	MPM3695-25
2	VCCBRAM/ VCCINT_IO	0.9V	±3%	3A	2	MPM3632C
3	VCCAUX/ADC	1.8V	±3%	3A	3	MPM3632C
4	VMGTAVTT	1.2V	±3%	7A	2	MPM3683-7
5	VMGTVCCAUX	1.8V	±3%	0.6A	3	MPM3606A
6	VMGTAVCC	0.9V	±3%	3A	1	MPM3632C
7	VCC_IO	3.3V	±3%	3A	4	MPM3632C
8	VCC_DDR	1.2V	±3%	3A	4	MPM3683-7
9	DDR_VTT	VCC_DDR/2	±3%	N/A	4	MP20075
10	DDR_VREF	VCC_DDR/2				

Zynq Ultrascale+ Reference Design Board

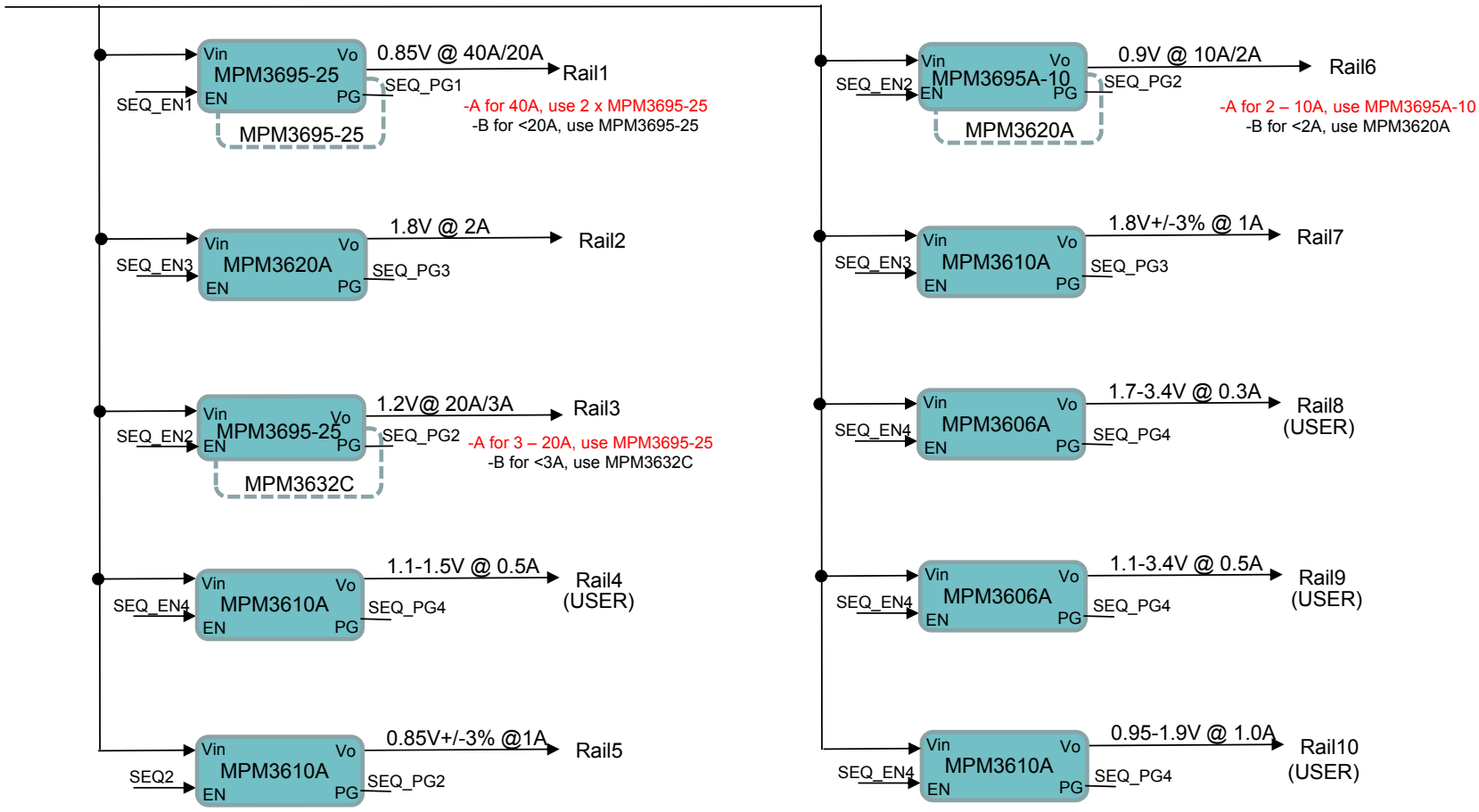


FPGA Series	FPGA P/N	EVB P/N	Core Current
Zynq Ultrascale+ MPSoC and RFSoC	ZU9CG, ZU9EG, ZU11EG-ZU19EG, ZU21DR to ZU29DR	EVREF0101-A	50A Max
	ZU3CG to ZU7EV	EVREF0101-B	25A Max

ZYNQ UltraScale+ FPGA Power Rails



MPS Power Module Solution Power Tree



Solution Summary – High Power Version

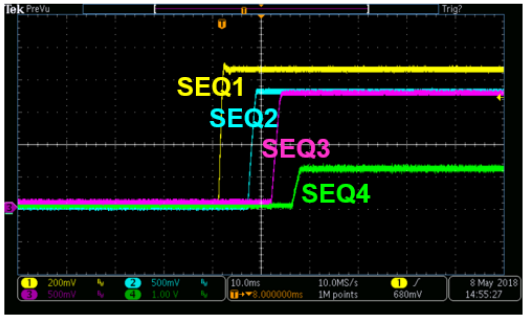
Rail Number	Rail Voltage	Maximum Rail DC Current	Part Number
1	0.85V	40A	MPM3695-25 x 2
2	1.8V	2A	MPM3620A
3	1.2V	20A	MPM3695-25
4	1.1V-1.5V	1A	MPM3610A
5	0.85V	1A	MPM3610A
6	0.9V	10A	MPM3695A-10
7	1.8V	1A	MPM3610A
8	1.7V – 3.4V	0.6A	MPM3606A
9	1.1V – 3.4V	0.6A	MPM3606A
10	0.95V - 1.9V	1A	MPM3610A

Solution Summary – Low Power Version

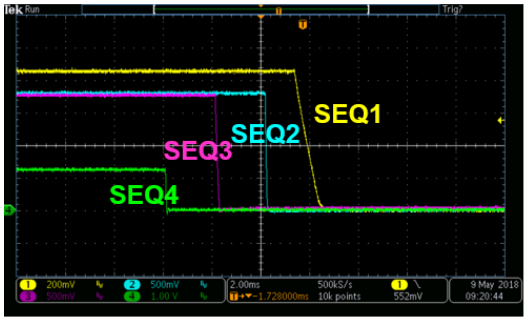
Rail Number	Rail Voltage	Maximum Rail DC Current	Part Number
1	0.85V	20A	MPM3695-25 x 1
2	1.8V	2A	MPM3620A
3	1.2V	3A	MPM3632C
4	1.1V-1.5V	1A	MPM3610A
5	0.85V	1A	MPM3610A
6	0.9V	2A	MPM3620A
7	1.8V	1A	MPM3610A
8	1.7V – 3.4V	0.6A	MPM3606A
9	1.1V – 3.4V	0.6A	MPM3606A
10	0.95V - 1.9V	1A	MPM3610A

Performance of Reference Designs Meet FPGA Specifications

Start-up Sequence

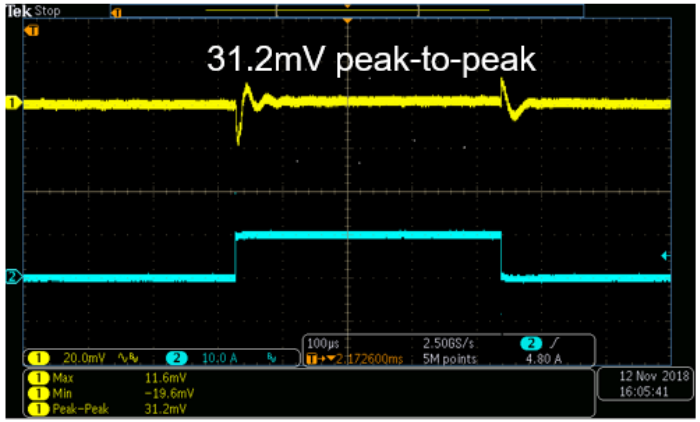


Shut-down Sequence



Monotonic start-up

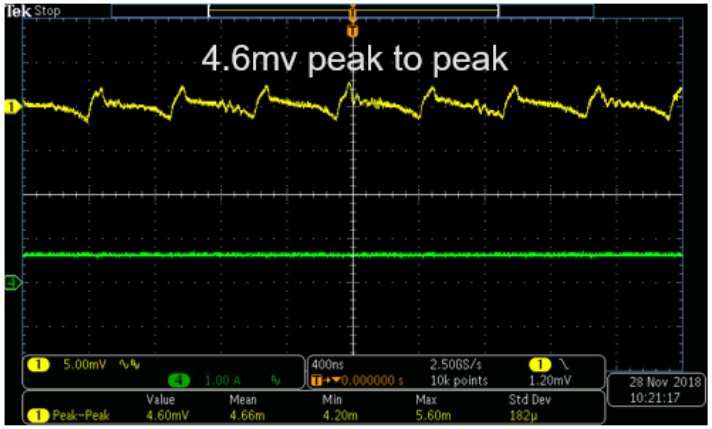
Load Transient Waveform
25% load step at 100A/us



100us/div

+-3% voltage deviation

Output Voltage Ripple at 0.6A Load



400ns/div

<10mV ripple for transceiver rails

Outline

Part I. Introduction

- Background
- Challenges in FPGA power solution design

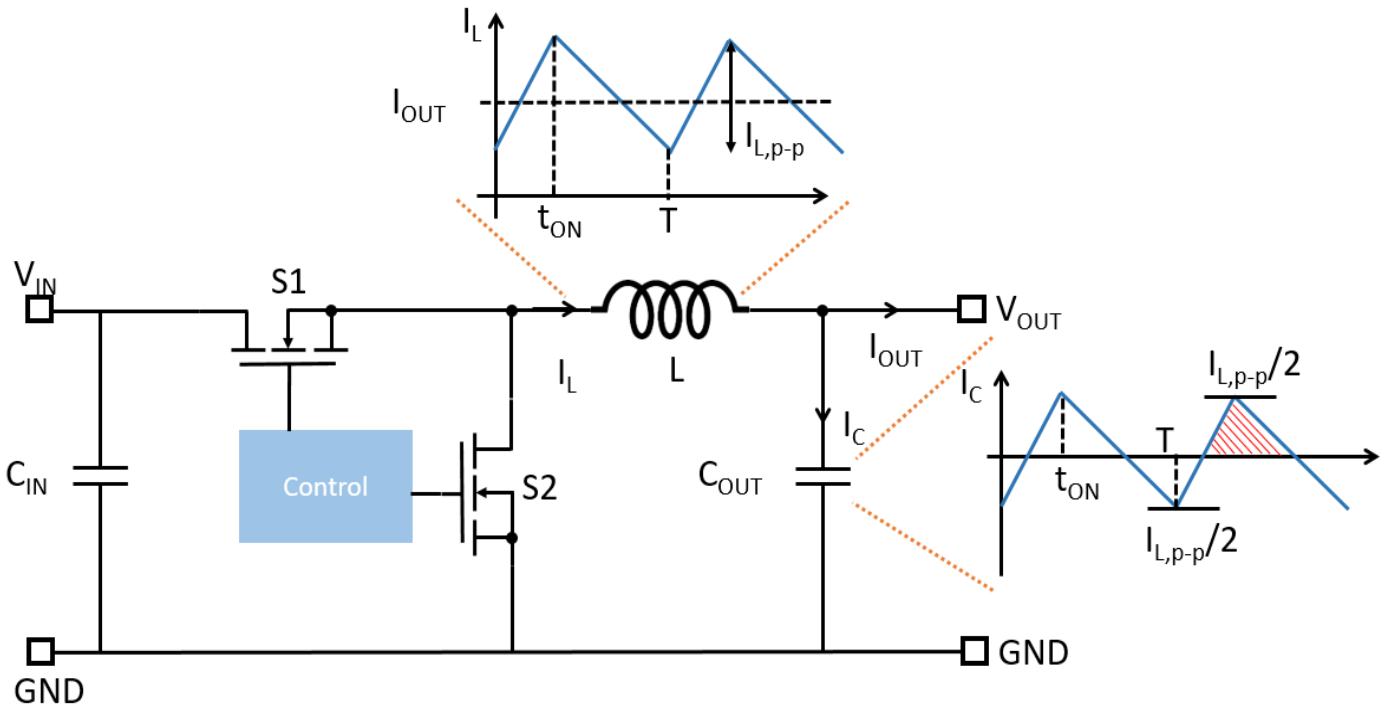
Part II. Optimum Design of FPGA Power Solution

- Power architecture of FPGA applications
- Typical requirement for FPGA power
- Advantage of power module solution
- Reference design with MPS power modules

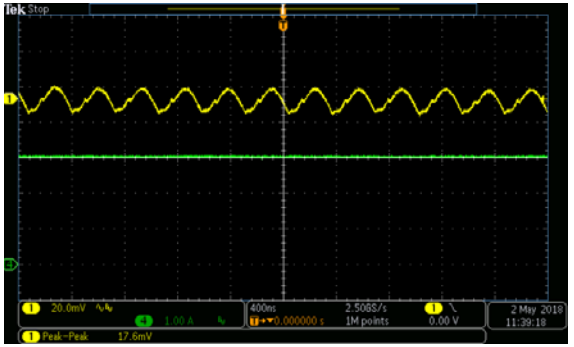
Part III. Replacing the LDO with Power Module

- Limitation of single stage filter
- Two-stage filter design

Forced CCM Operation

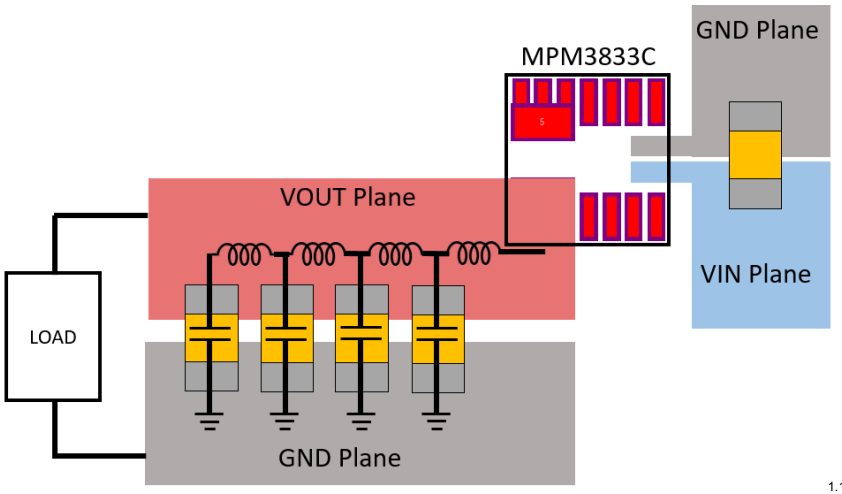


Add more bypass capacitors to reduce output voltage ripple

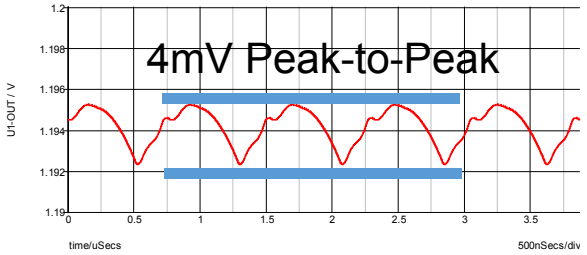


$$C_{Min} = \frac{I_{L,p-p}}{8 f_{SW} \Delta V_{C,p-p}}$$

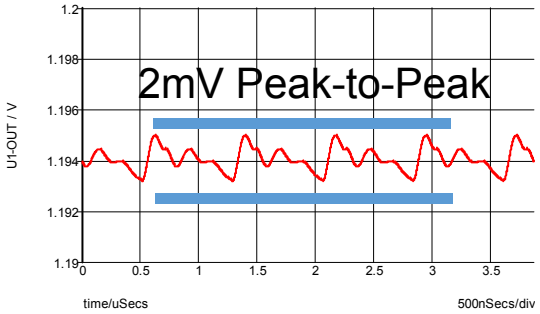
Why use second stage inductive filter?



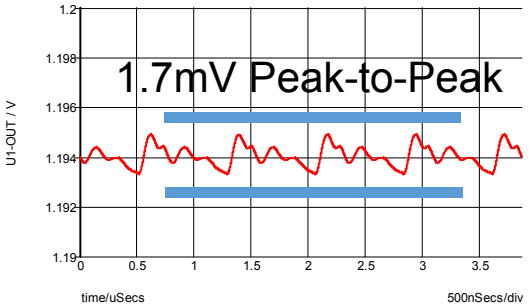
Output voltage ripple with one 22uF output capacitor



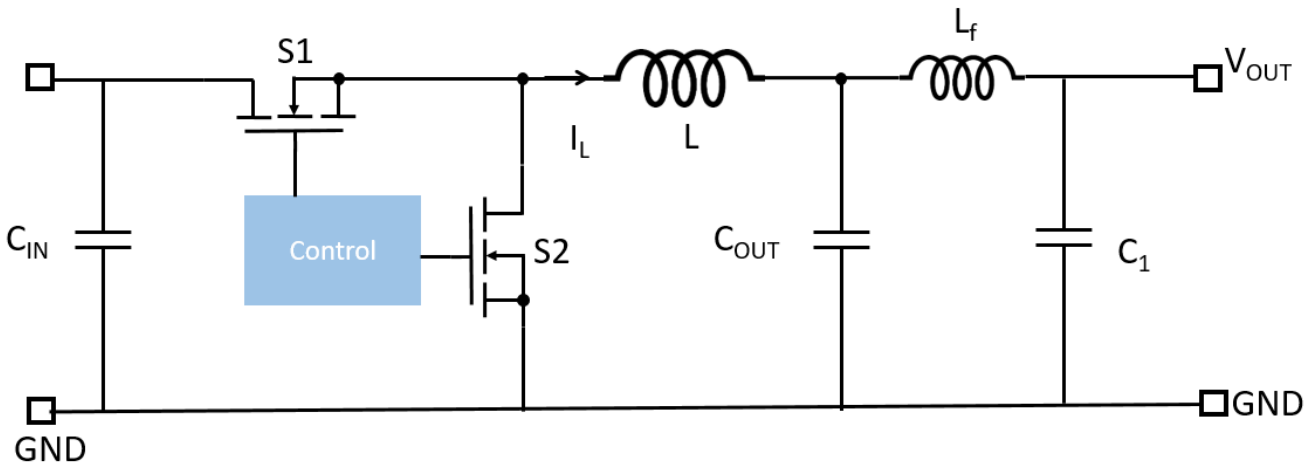
4x22uF output capacitor



5x22uF output capacitor



Design the Second Stage Filter



Design COUT to reduce the output voltage ripple to 5mV-10mV

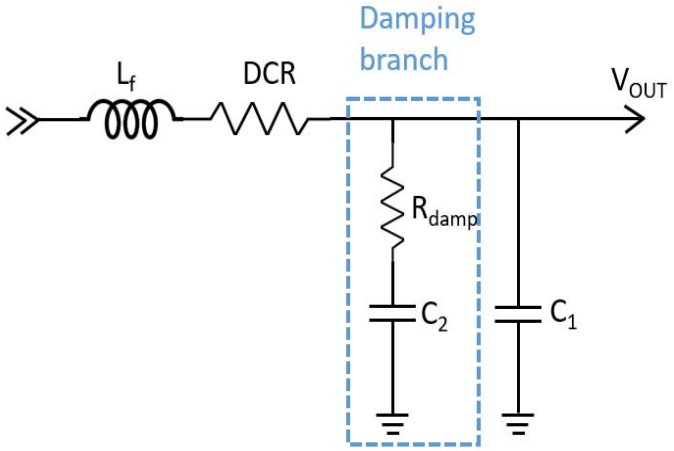
Select L_f at 0.22uH-1uH value

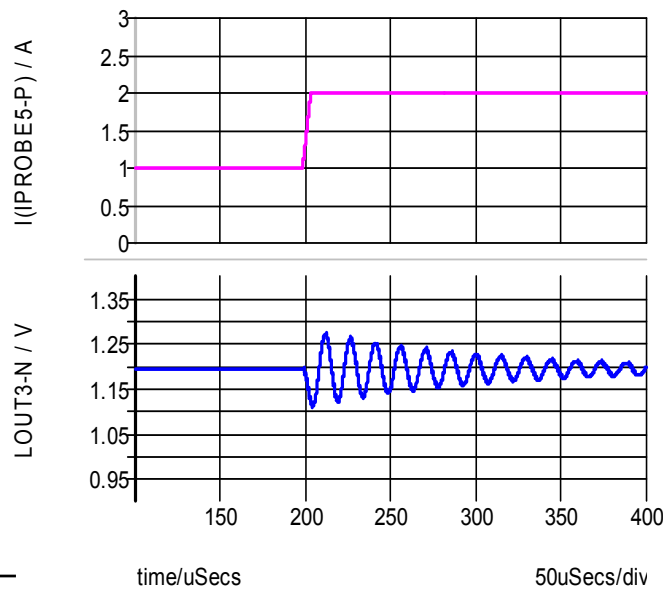
$$C_1 = \frac{1}{4\pi^2 f_0^2 L_f}$$

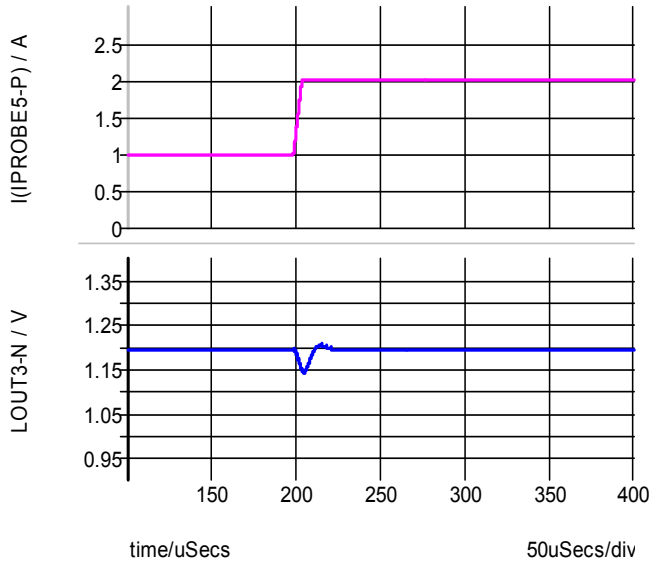
$$f_0 = \frac{f}{10^{\frac{20log\frac{V_{O,p-p}}{V_{1,p-p}}}{-40}}}$$

https://www.monolithicpower.com/cn/passive-filter-design-concept-of-buck-regulators-for-ultra-low-noise-applications

Damping of the LC filter





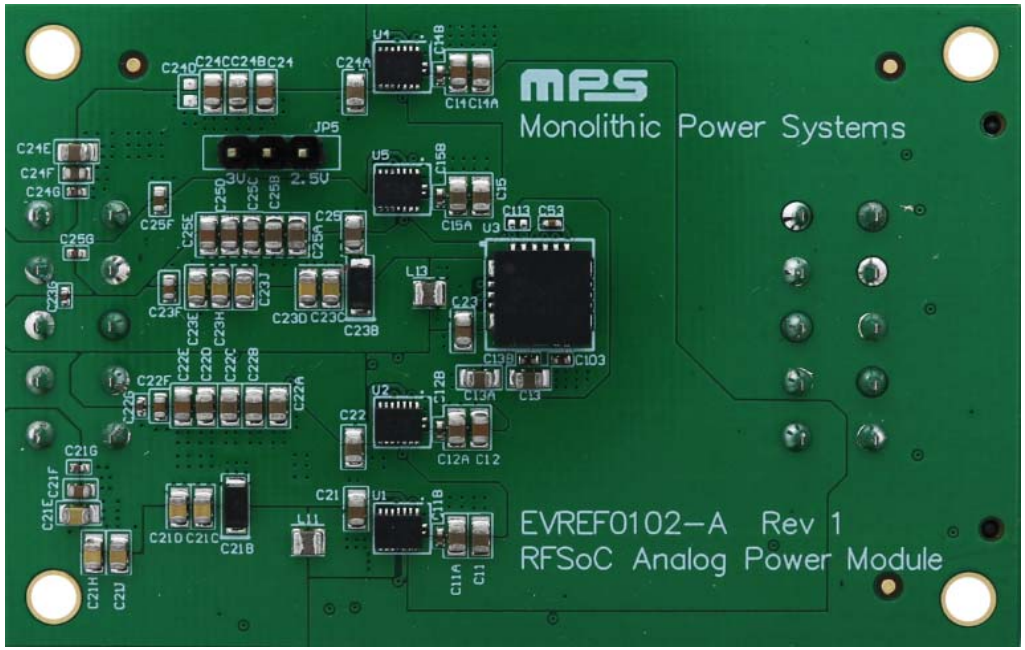


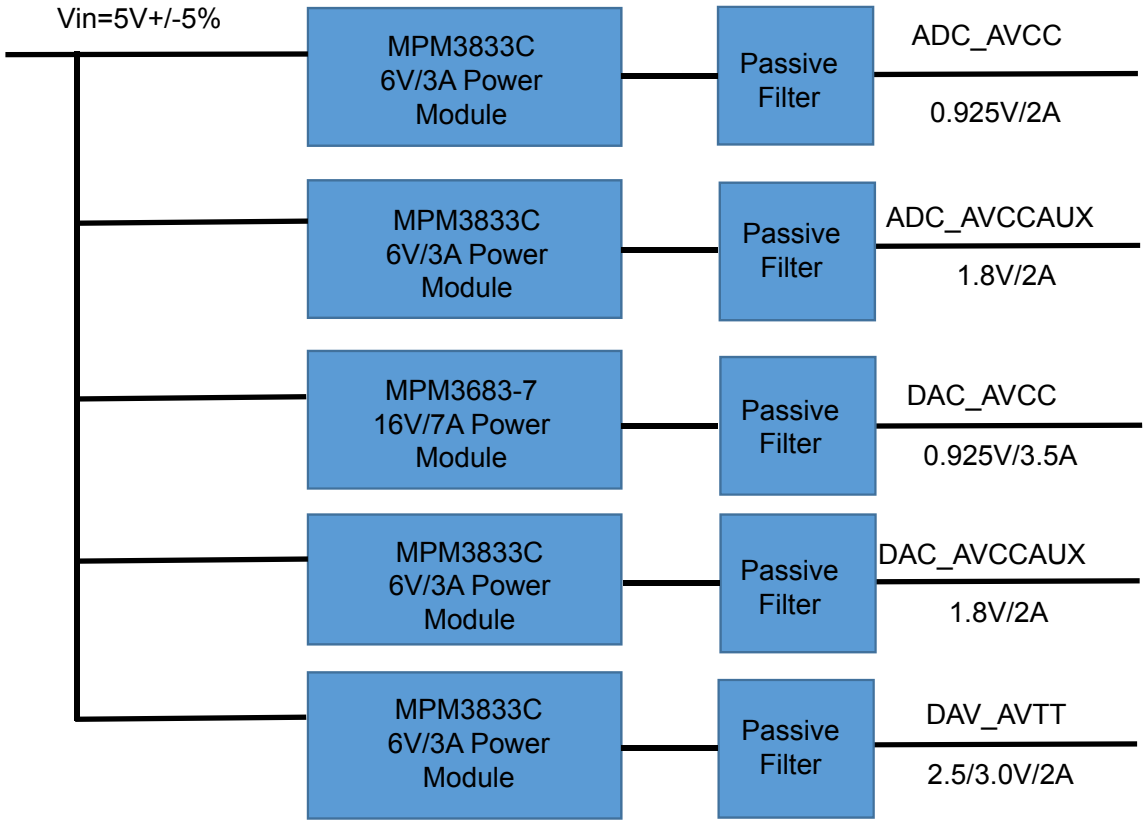
Need to satisfy

$$R_{Damp} > 2\sqrt{\frac{L_f}{C_2}}$$

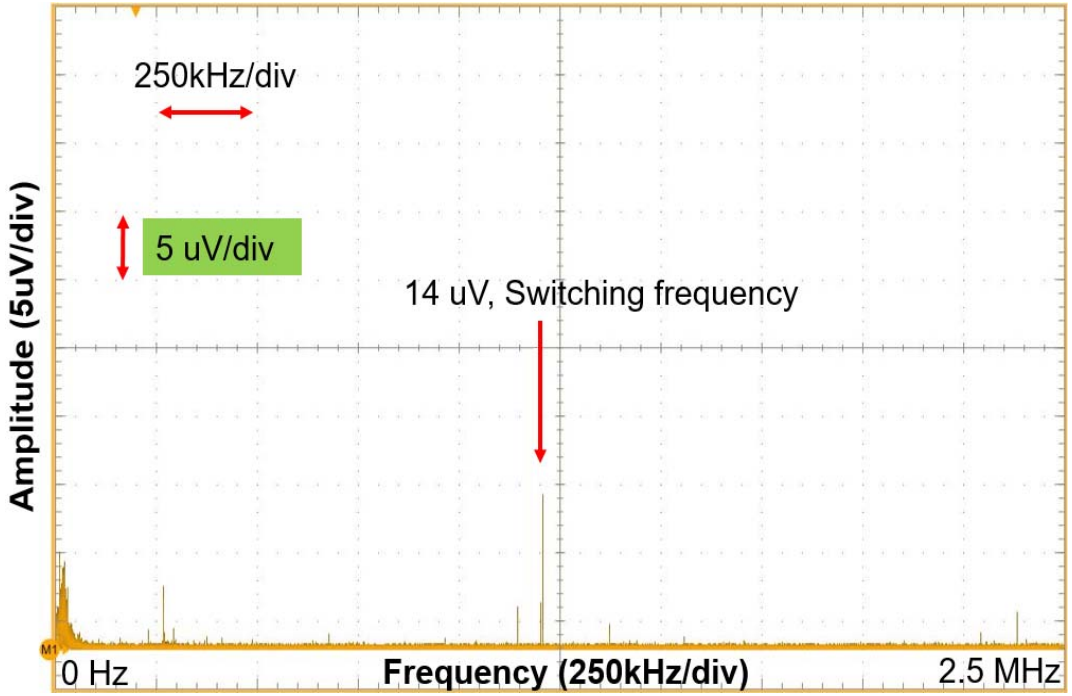
$$R_{Damp} < 0.5\sqrt{\frac{L_f}{C_1}}$$

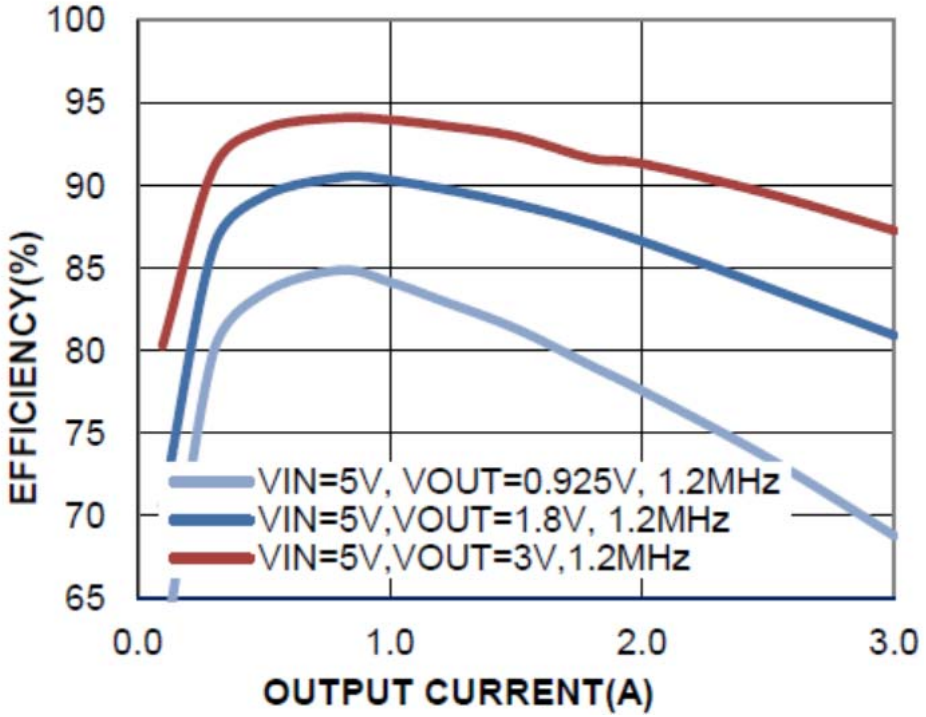
Same Performance as LDO Solution





Same Noise Performance as LDO





4X more efficient than LDO

Contact Information

For more information regarding MPS reference designs, please contact referencedesign@monolithicpower.com

Or Heng Yang Heng.Yang@monolithicpower.com

Complete Reference Design Available at:
https://www.xilinx.com/products/technology/power.html#partners and
https://www.monolithicpower.com/en/design-tools/reference-design-partners/xilinx-reference-design.html

Thanks!