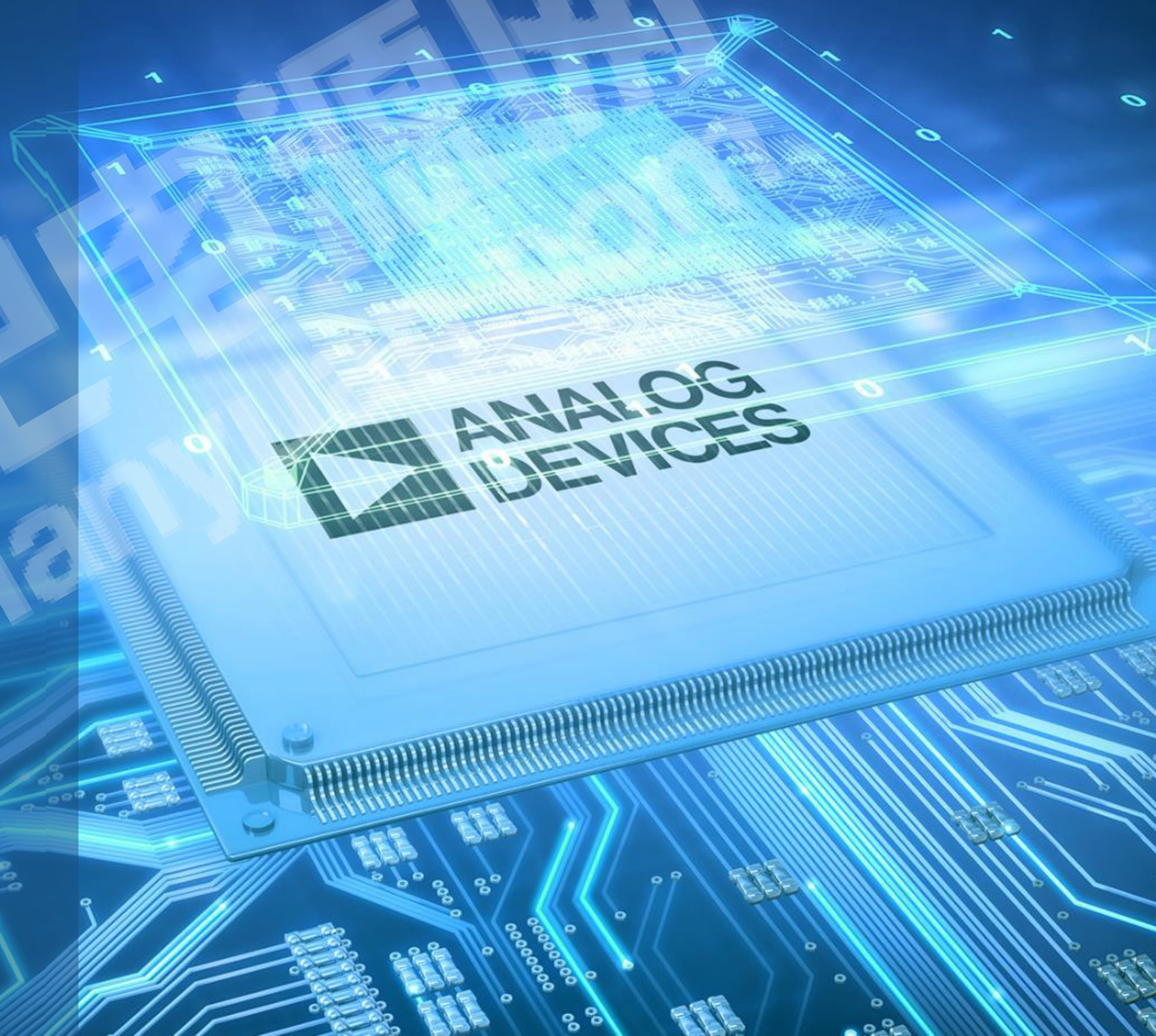
# ADI Power Products Make EMI Design Easier




FRANK DU

POWER APPLICATION ENGINEER

Sep. 2019

# Outline

- Some EMI Basic
- ADI Low EMI Products
- ISO Modules EMI Test

# Introduction To EMC

General EMC Certification Mark

EU(EMC)

China(EMC)

USA(EMI)

Japan(EMI)

Australia(EMI)

Taiwan BSMI(EMI)

Mexico(EMI)

Korea(EMC)

# EMI - Conducted vs. Radiated

**EMI** (Electro Magnetic Interference)

**Conducted (<30MHz)**
FCC: 150kHz-30MHz

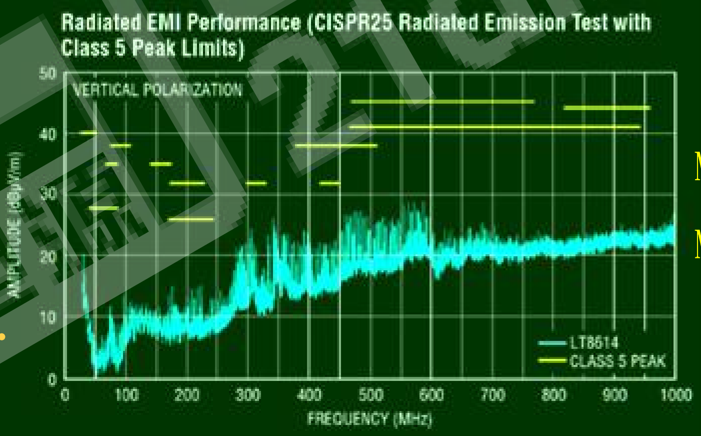
- **Differential Mode (DM)**
- Common Mode (CM)

Lower order harmonics are NOT sensitive to supply parasitic and can be estimated with LTpowerCAD.

**Radiated (>30MHz)**
FCC: 30MHz-1GHz

- Magnetic
- Electric

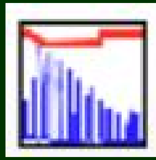
"Silent Switcher" helps!

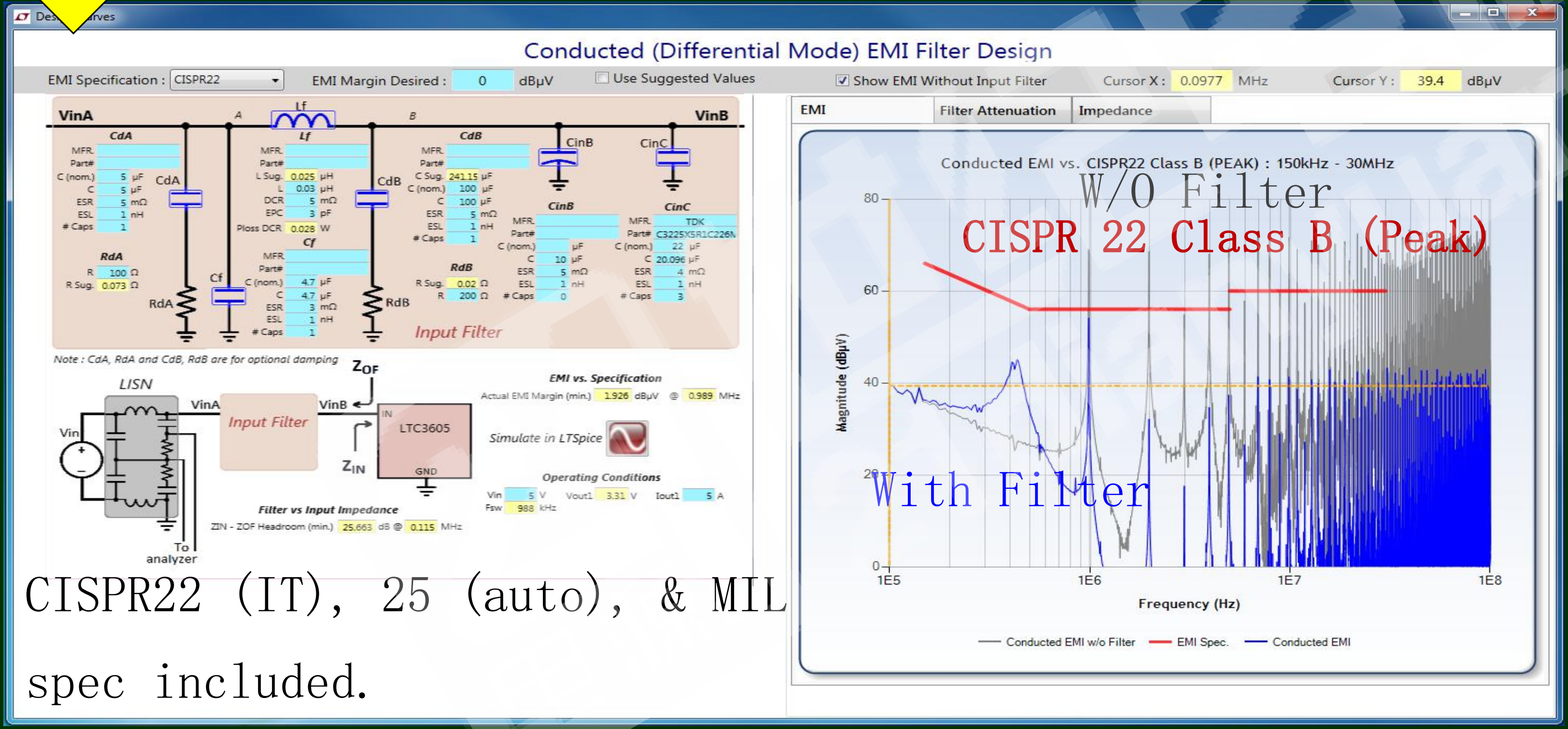



Minimum hot loop

Magnetic cancellation

# DM EMI Filter Design in LTpowerCAD



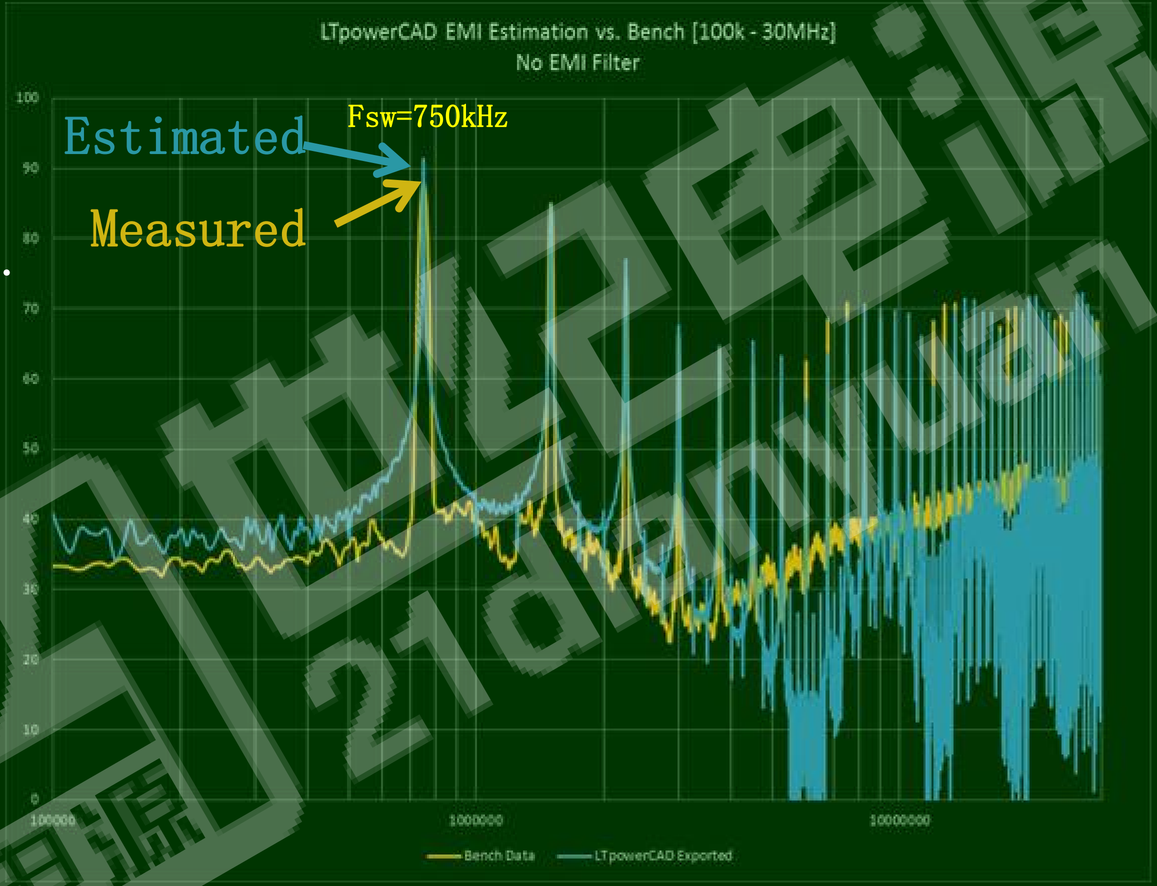



- First few orders of $f_{SW}$ harmonics determine the filter size.

# Estimated vs. Measured EMI Data (1)

## 1. Without EMI filter

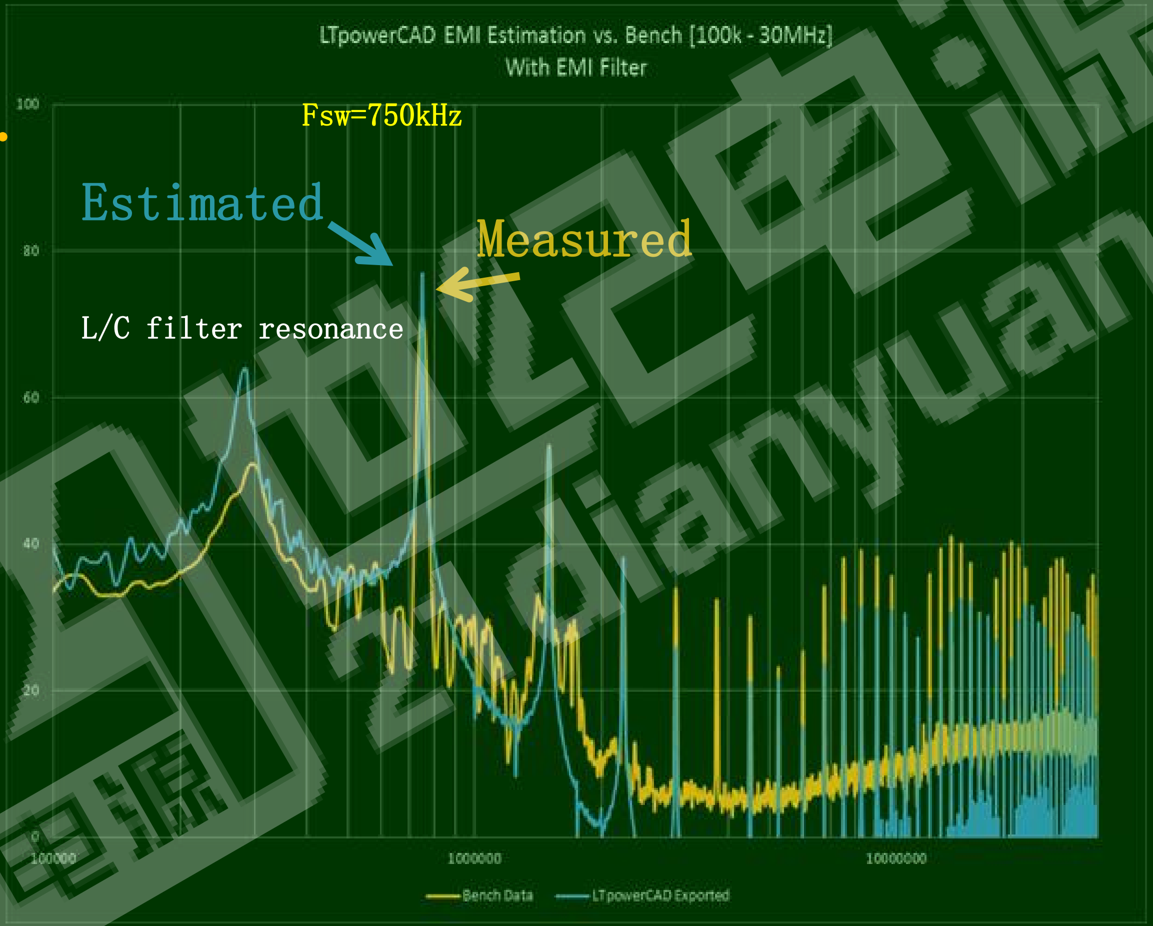
- LTC3851A single phase buck demo board. (12Vin to 1.5Vo/15A, 750kHz).
- Good matching of peak values.
  - First few orders of $f_{SW}$ harmonics.
  - Measured data are slightly lower.



# Estimated vs. Measured EMI Data (2)

## 2. With input EMI filter

- Good matching of peak values.
  - First few orders of $f_{SW}$ harmonics.
  - Measurement slightly lower.
- Additional peak at lower frequency
  - Caused by filter L/C resonance.



# Introduction To EMC

LISN(Line Impedance Stability Network)

Impedance at 150KHZ

1uF: 1.06ohm

50uH: 47ohm

(DC pass, HF block)

100nF:10.6ohm

(DC block, HF pass)

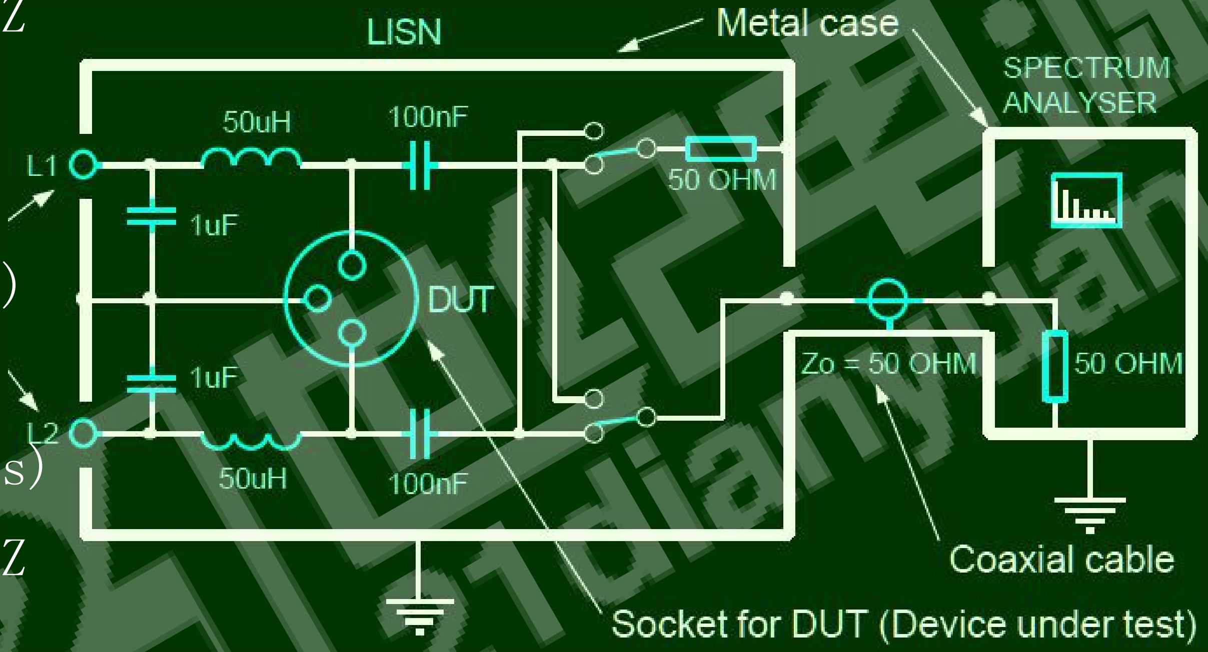
Impedance at 1.5MHZ

1uF: 0.106ohm

50uH: 470ohm

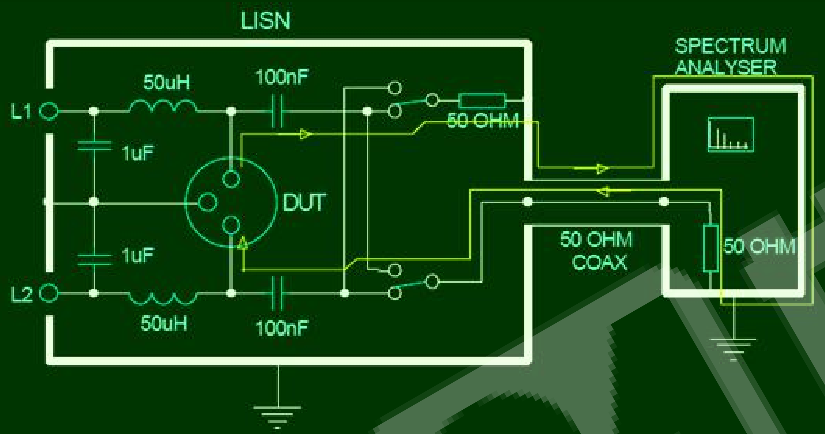
100nF:1.06ohm

50ohm dominate at high frequency

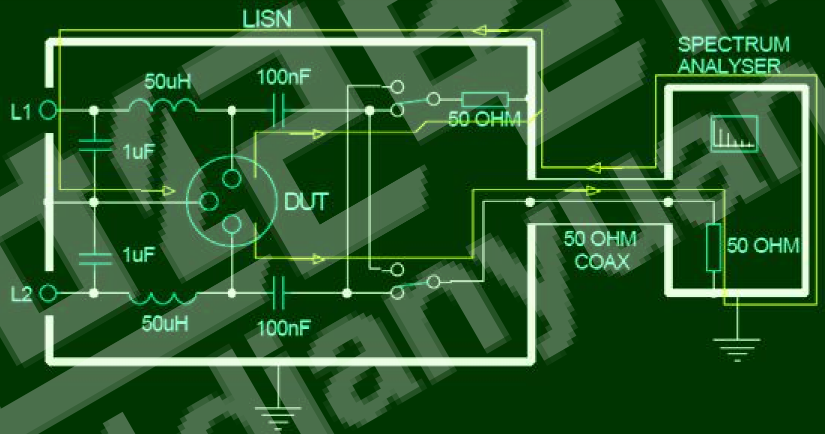


# How to measure CE?

Differential Mode noise




Common Mode noise




Total line impedance

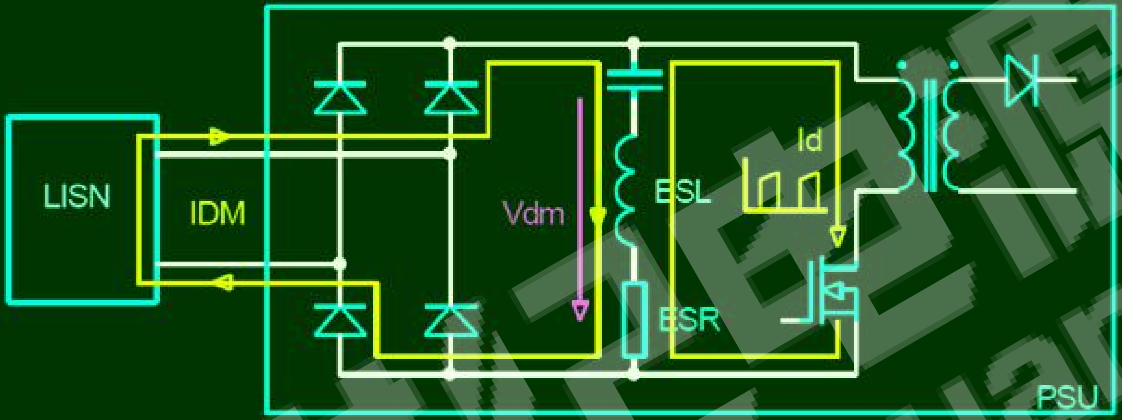
100ohm（50+50）

Total line impedance

25ohm （50//50）

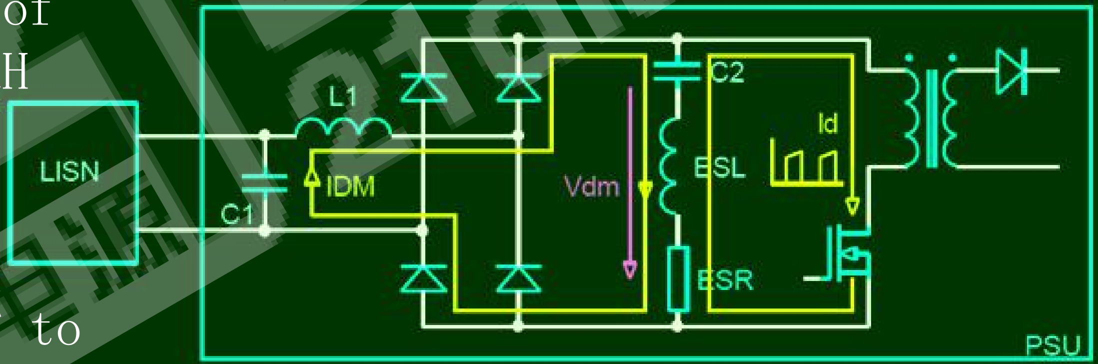
# Differential Mode Path and Filter

- Understand differential mode current
- Vdm depends on ESL, ESR and di/dt
- 100ohm in LISN dominate



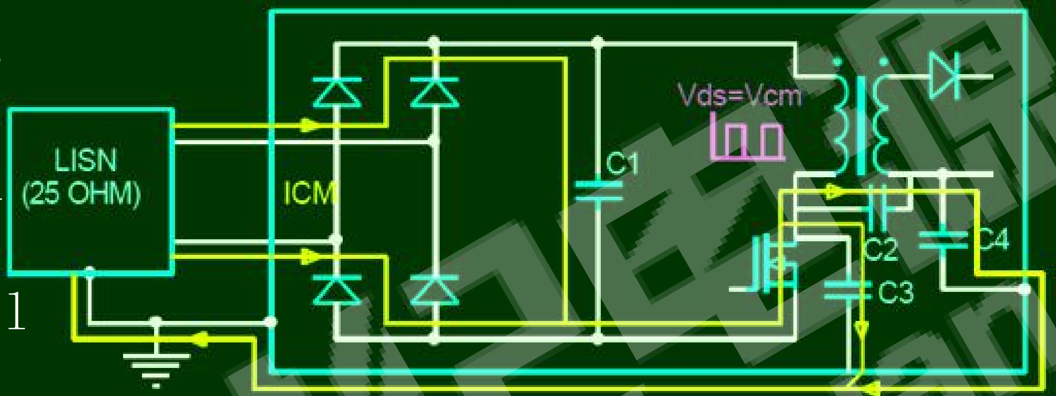

Add differential Mode filter

- L1C1 form low frequency pass filter
- L1 range from tens of uH to hundreds of uH
- L1 usually leakage inductor of common choke
- C1 range from 0.1uF to 1uF (low ESR、ESL)

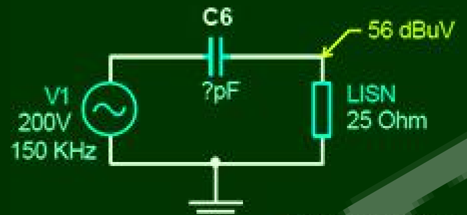


# Common Mode Path and Filter

- Understand common mode current(high dv/dt)
- Drain to safety ground parasitic cap(C3,C2)
- Very few parasitic will cause EMI over spec



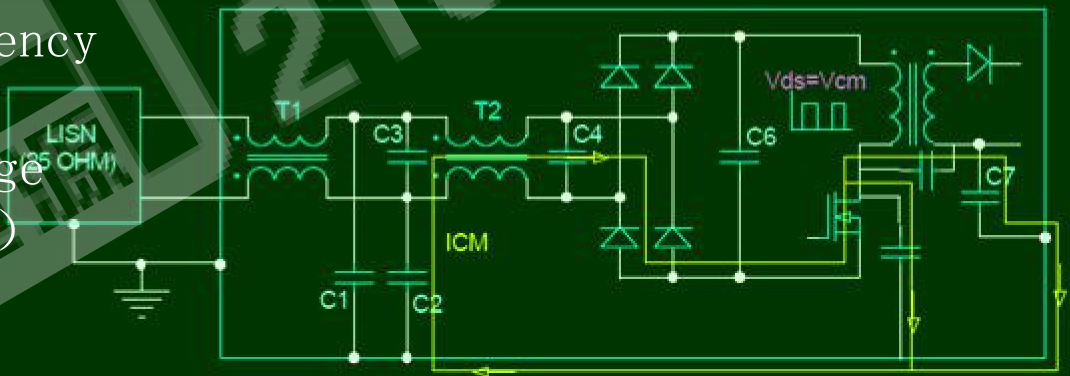

Only 0.067pF!!!!




Equivalent circuit

Add common mode filter

- T2C1C2 form low frequency pass filter
- C1C2 will cause leakage current (1nF to 4.7nF)
- T1T2 range from1mH to 10mH






ANALOG DEVICES
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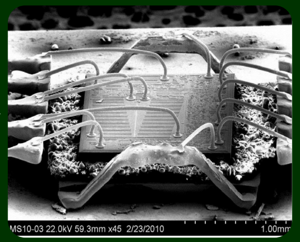
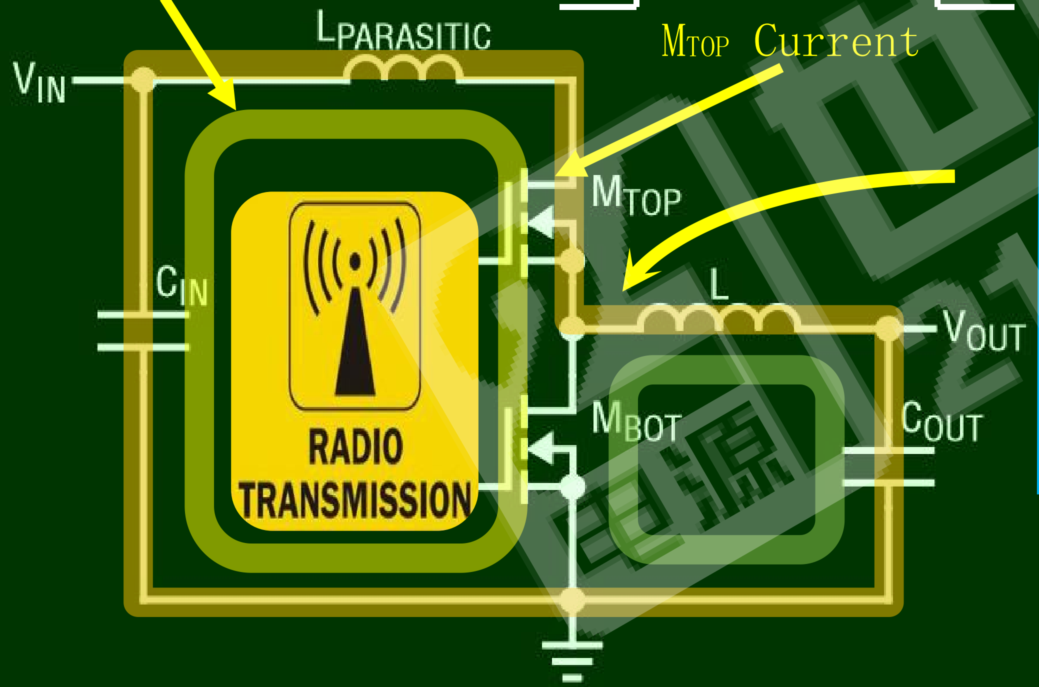
# How does a BUCK Affect EMI?

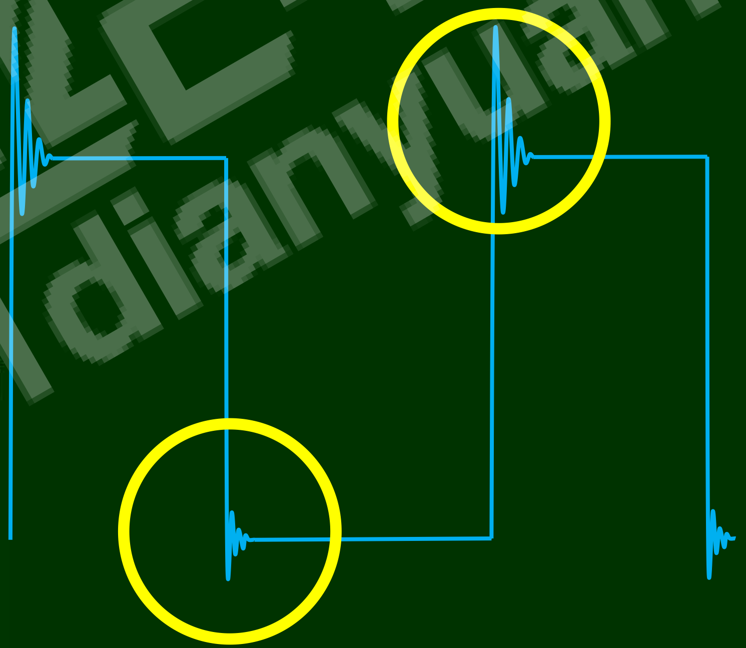
Parasitic inductance due to copper traces, bond wires, ESL of capacitors and FET internal metal




Excessive rings at the switching edges cause conductive noise and radiation

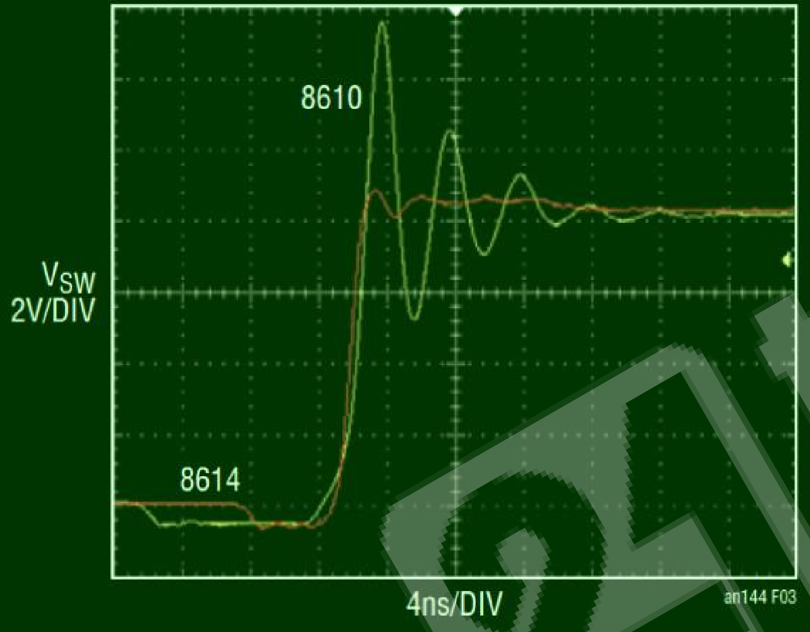
High dI/dt
"Hot Loop"



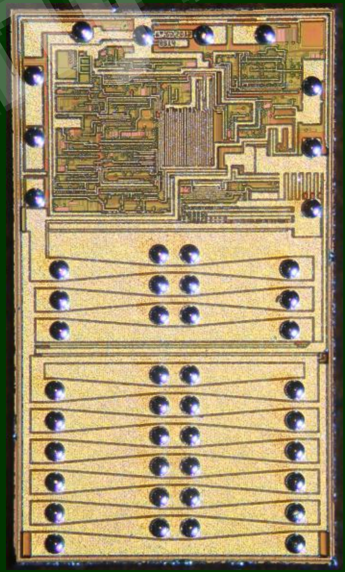
# Copper Pillar Flip Chip for Lower ESL and ESR

## Silent Switcher 1

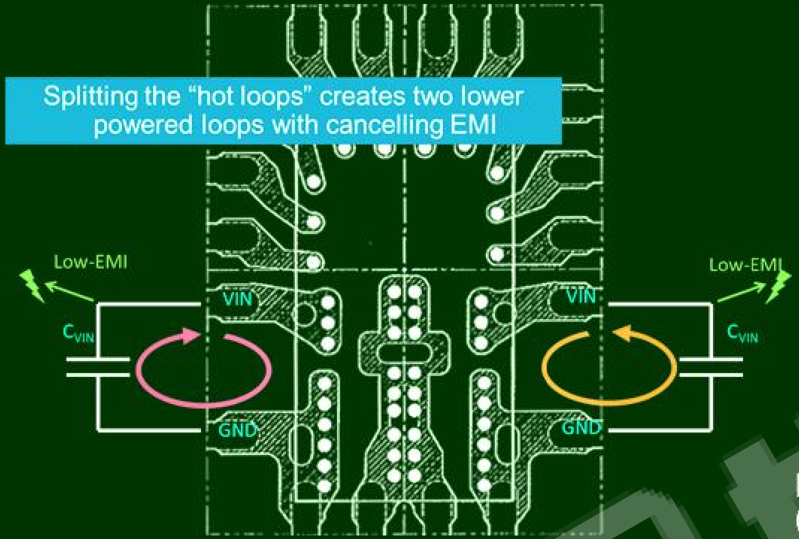


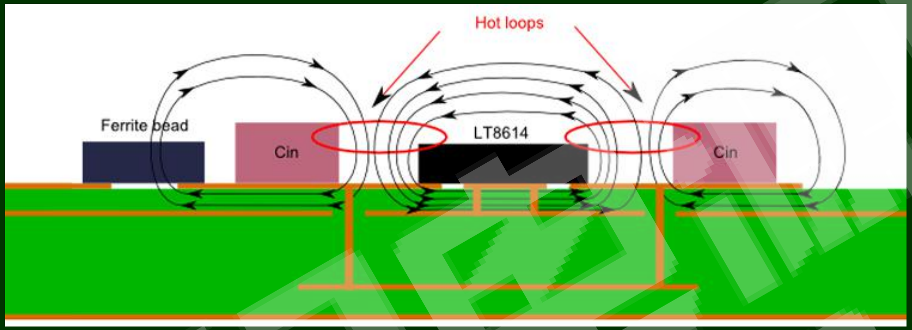

LT8610: non-silent switcher
Bond wires in MS16E
No magnetic cancellation

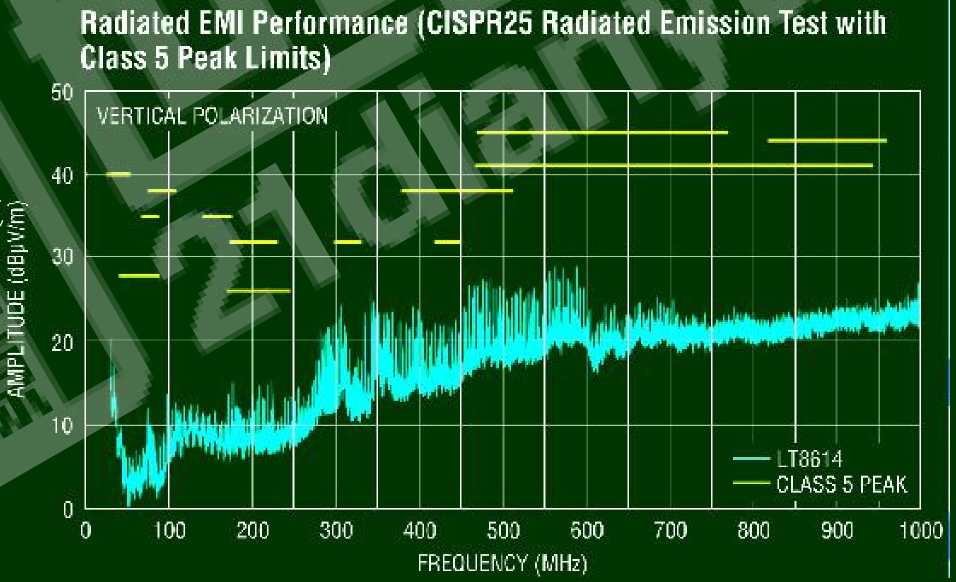

LT8614: Silent Switcher 1 Magnetic cancellation
+ CuPillar Flip-Chip
Fast edge rate, minus the EMI ringing on the switch node.



# Innovation - Silent Switcher



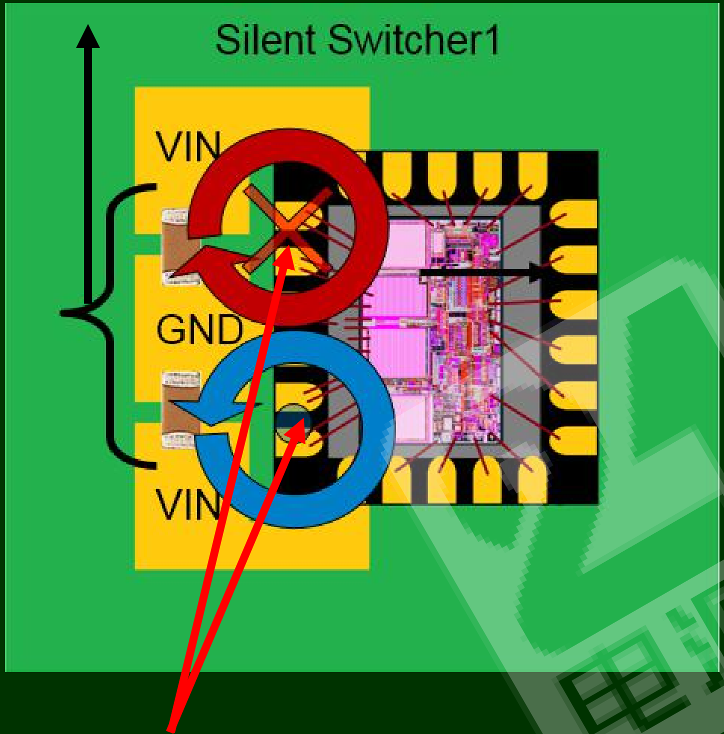



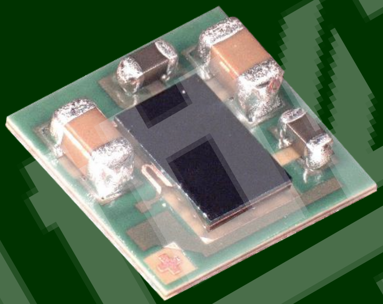

- The two high current loops cancel each others magnetic field, almost like enclosing the circuit in a metal box

# Magnetic Field Cancellation Loops on the Silent Switcher

Dual local bypass capacitors are mounted close to the IC package on the PCB.

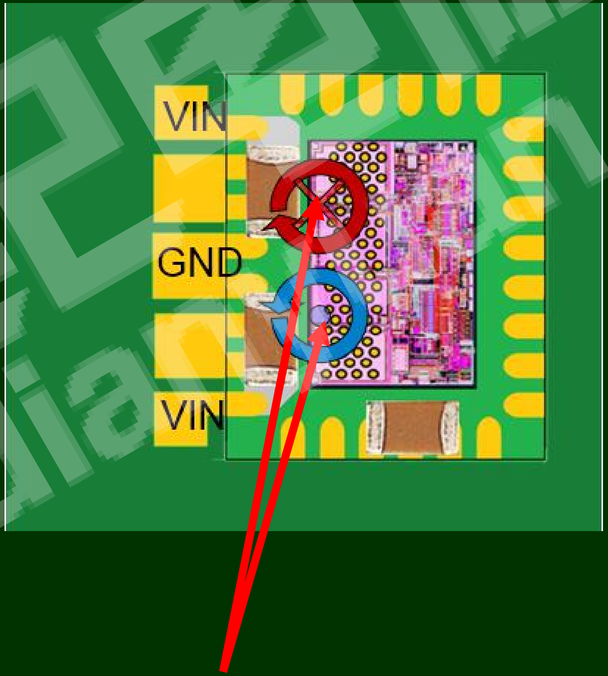



magnetic loop diameter = 0.5cm



All high di/dt stays in package: customer PCB layout is now <u>non-critical</u>

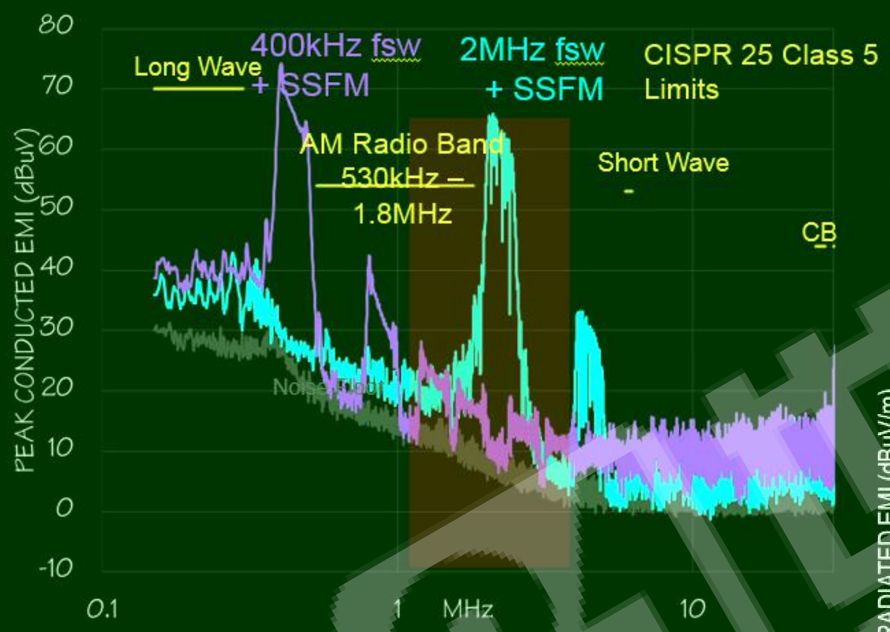
Silent Switcher2



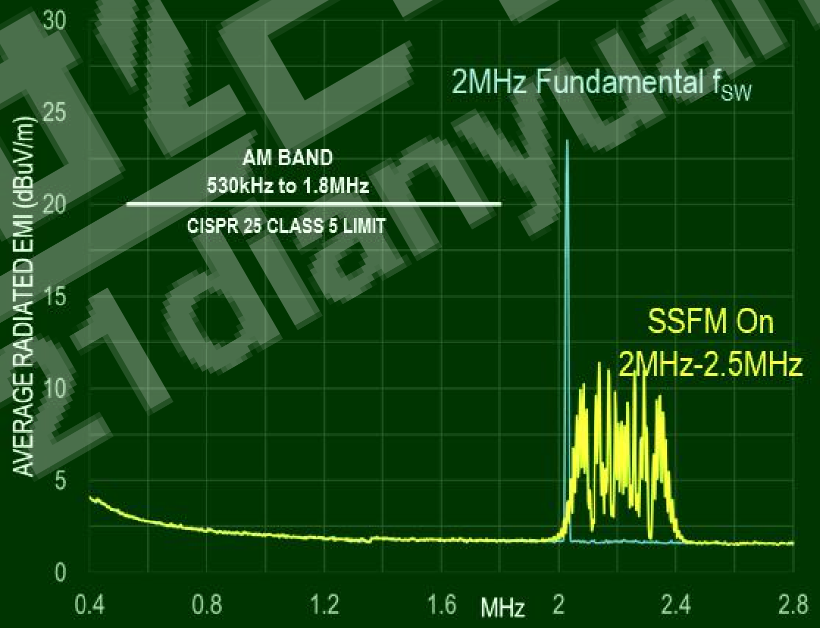

magnetic loop diameter = 0.1cm

# Frequency Selection and SSFM

correct switching frequency selection

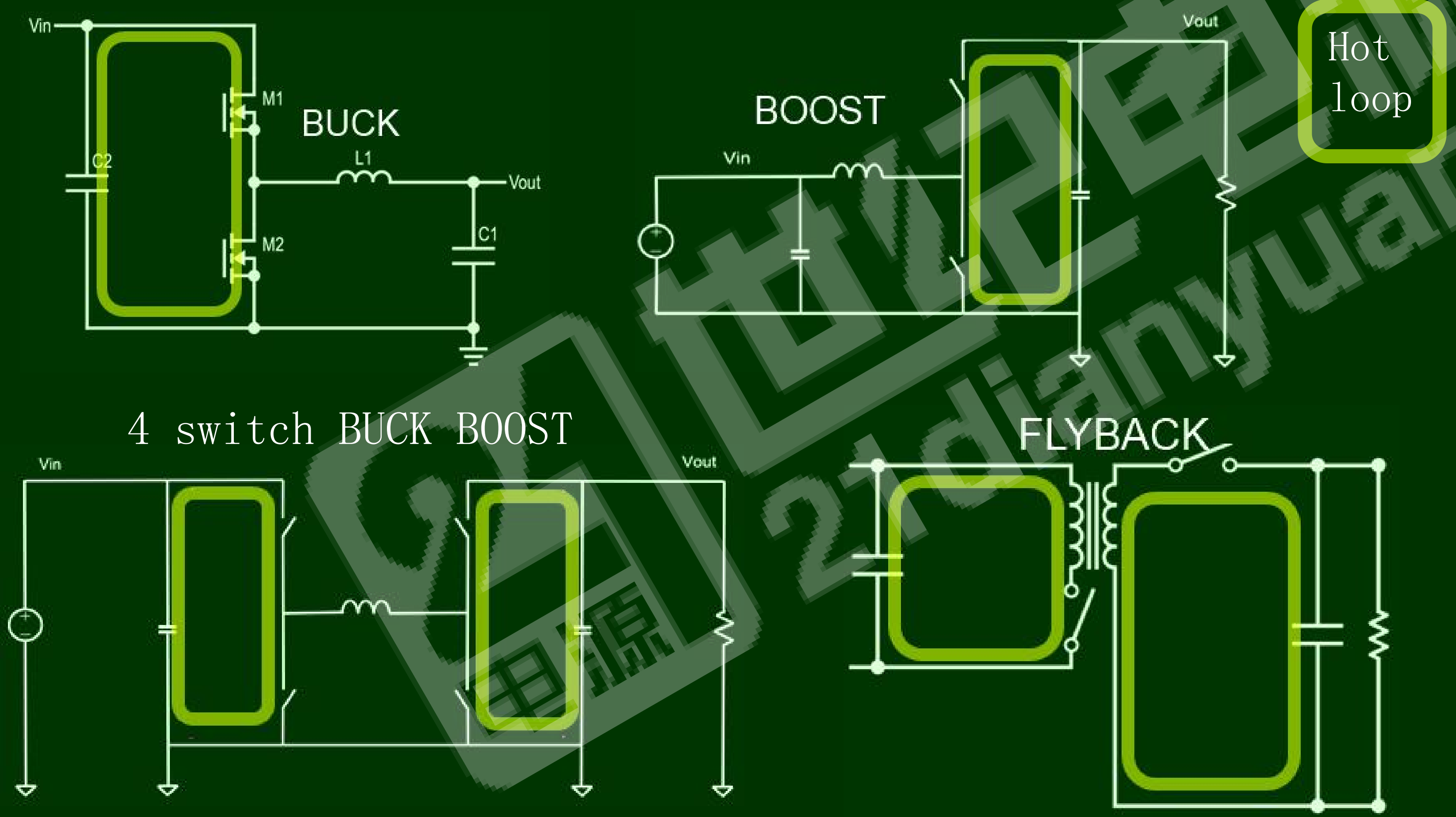



SSFM spreads the fundamental and all of its harmonics for reduced EMI measurements.



# Identifying Topology Hot Loops

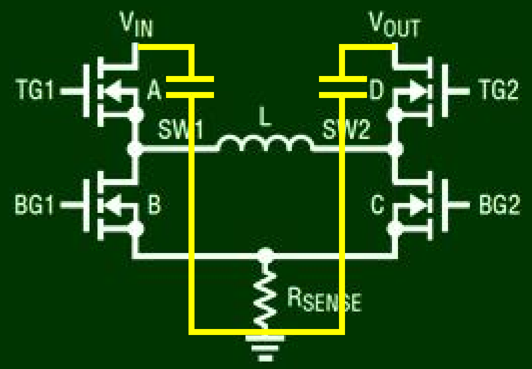
- Identify topology hot loop, and keep hot loop as small as possible!
- Hot loop magnetic cancellation will help reduce EMI radiation!



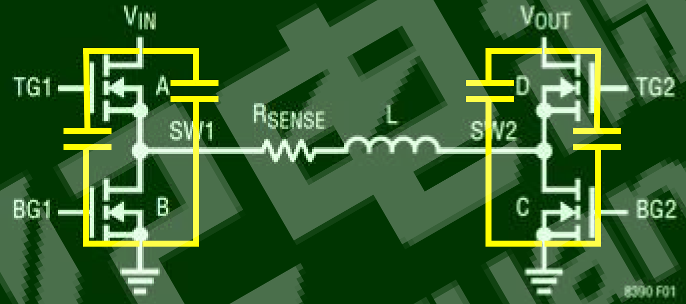
# EMI Performance - LT3790 vs LT8390/90A

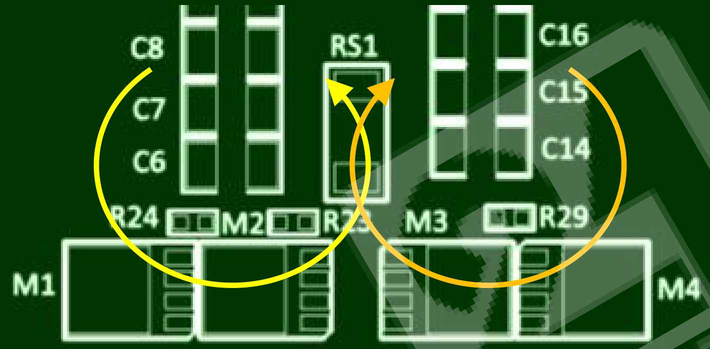
Low EMI

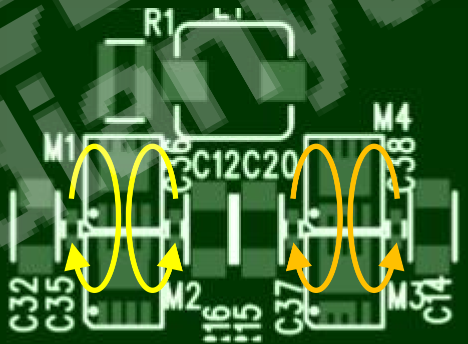
## LT3790
Ground Current Sense




## LT8390/90A
Inductor Current Sense



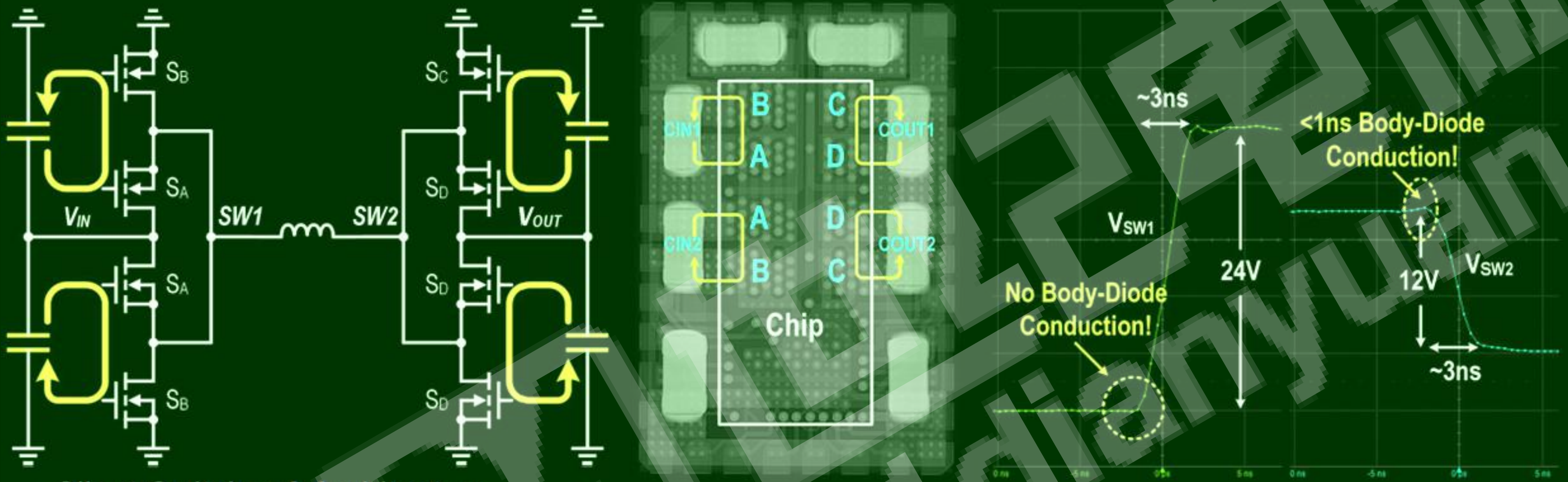




Single big hot loop
for both $V_{IN}$ and $V_{OUT}$

“Silent Switcher” style
small dual hot loops for both $V_{IN}$ and $V_{OUT}$

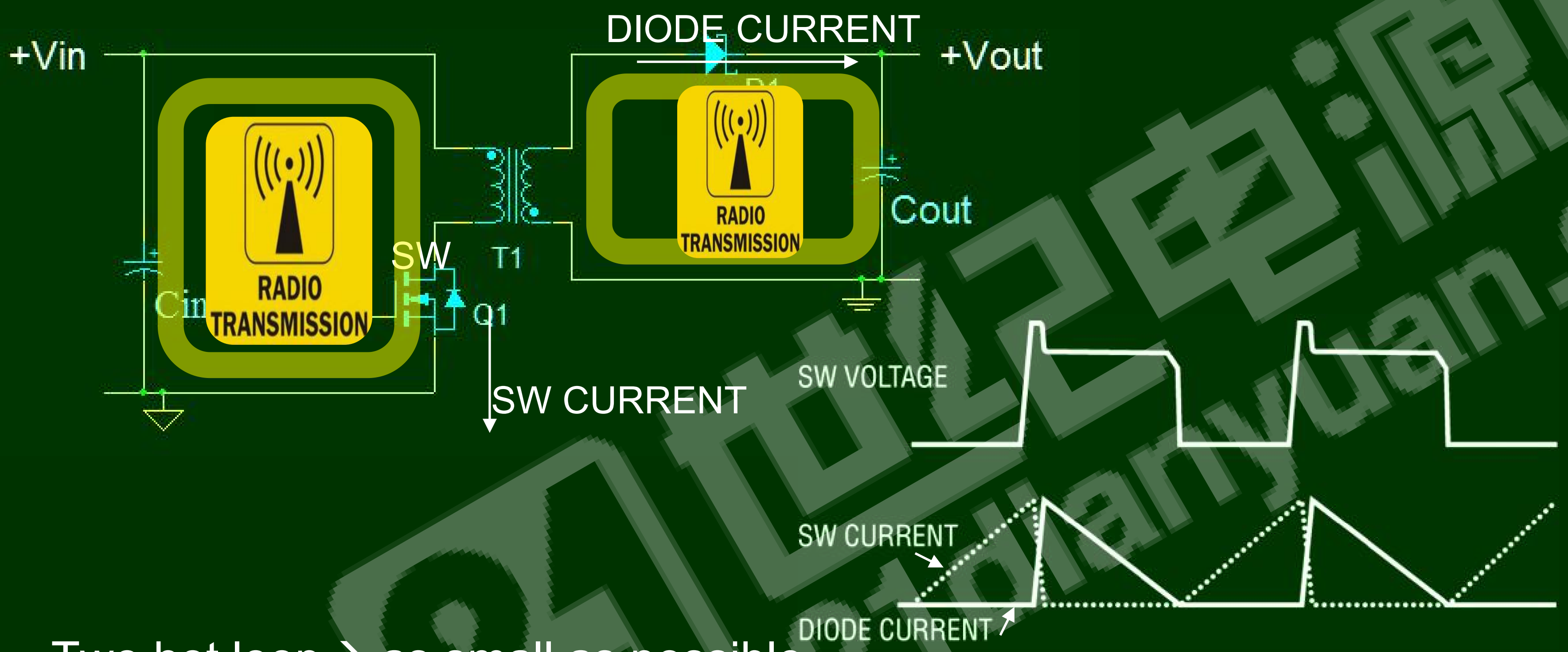
# Silent Switcher 2 Architecture for Monolithic Buck-Boost




- Silent Switcher 2 Architecture
  - Symmetrical hot loops
  - Internal hot loop caps
  - Cu pillars instead of bond wire
- Safe zero dead time

For Low EMI, High Efficiency, Simple PCB

# How does a Flyback Converter Affect EMI?



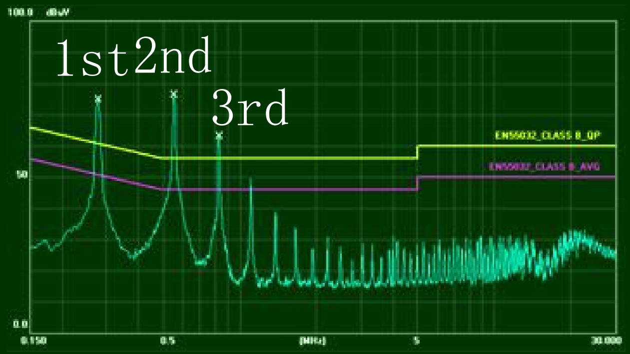

Two hot loop→ as small as possible

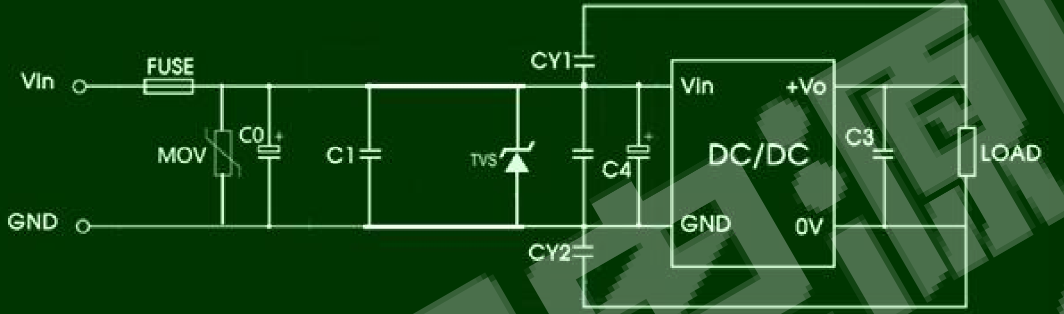
Boundary mode→ small diode reverse recovery

Common noise→ SW node ringing, parasitic capacitance, YCAP

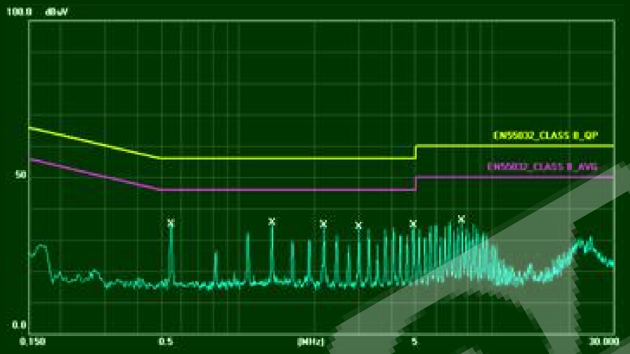
Differential noise→ input cap, LC filter

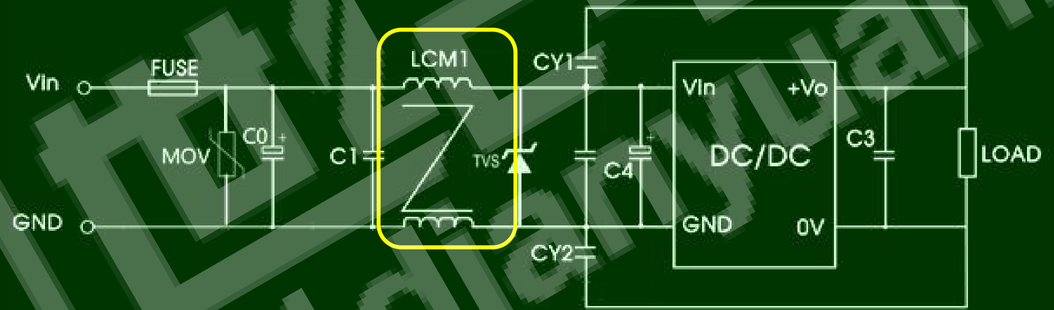
# AP0624D05LY Conducted Emission



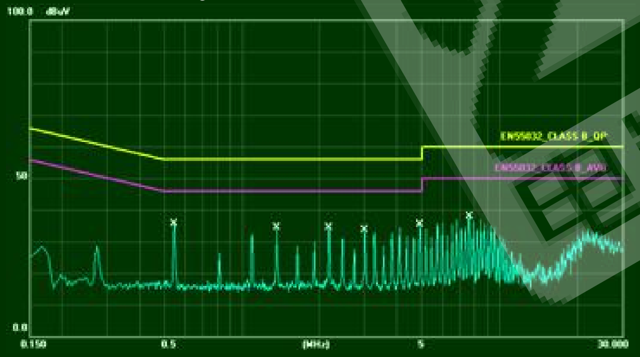



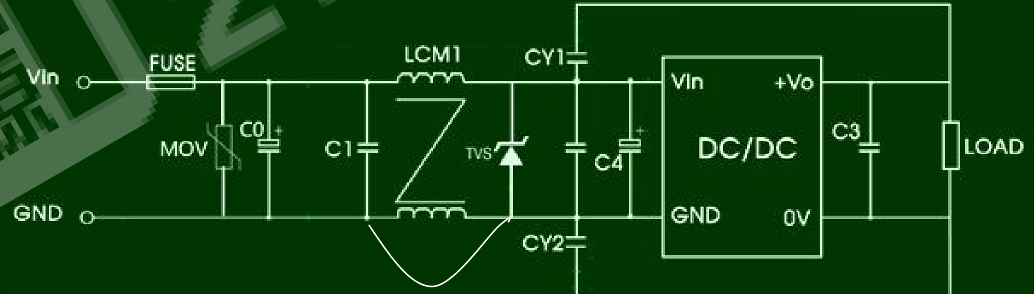

2mH CM choke



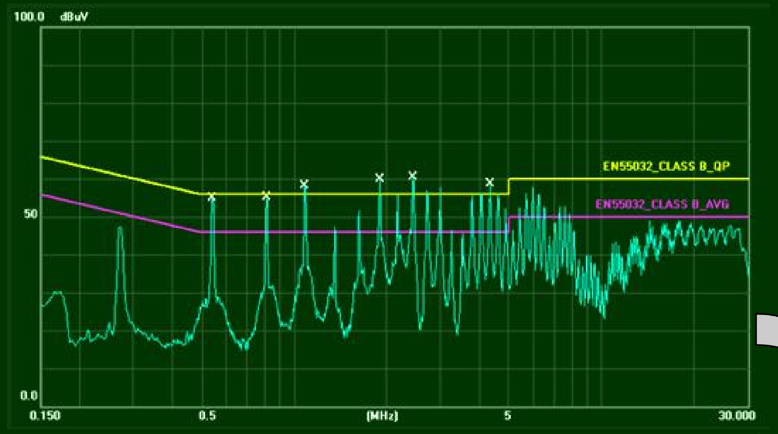



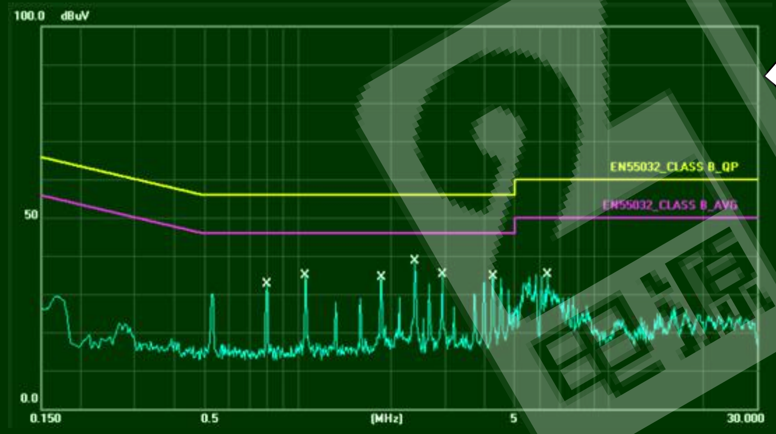

Why common choke have effect on low frequency differential noise?



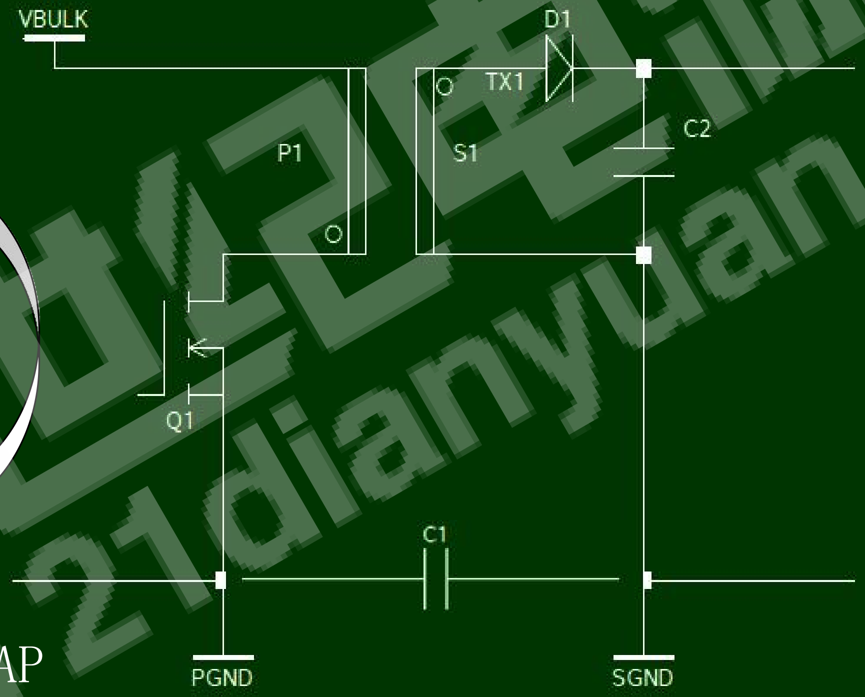
# AP0624D05LY Conducted Emission




YCAP

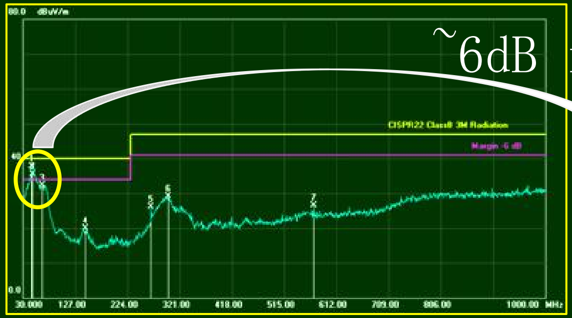
Effect



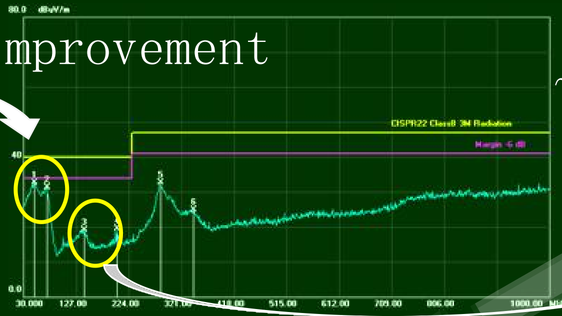
# AP0624S05LY Radiated Emission

~6dB improvement

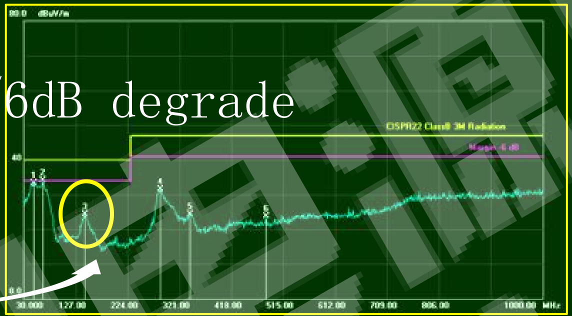
~6dB degrade



C1,C2,C3 far away

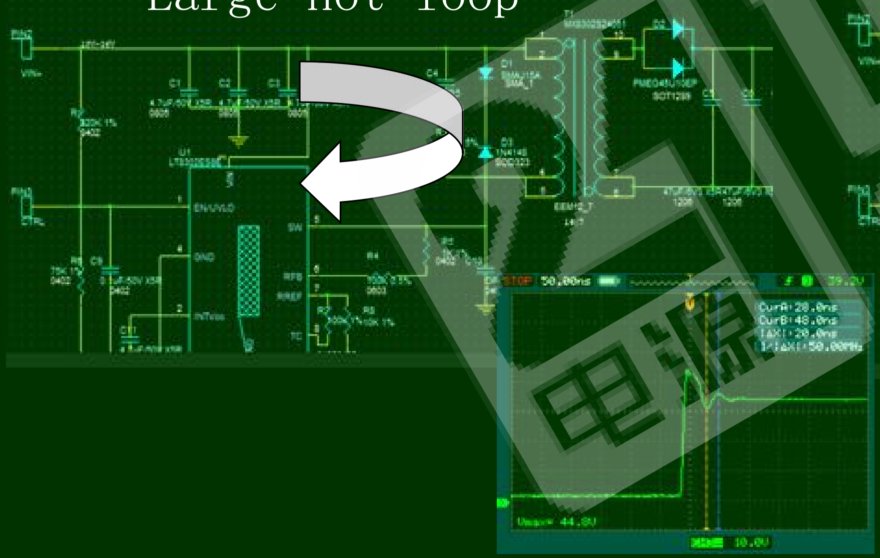


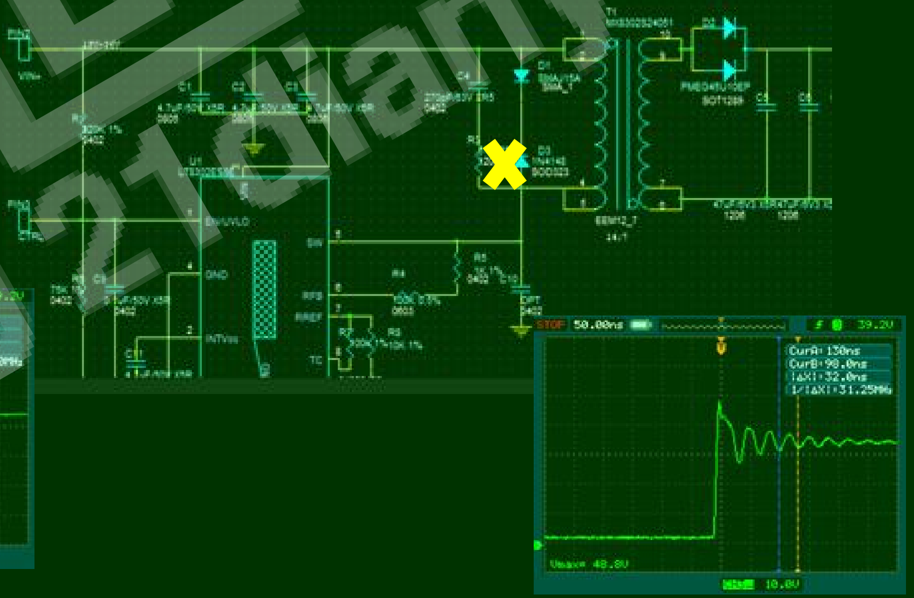
Put C1,C2,C3 close to T1 and U1



No RC snubber

Large hot loop

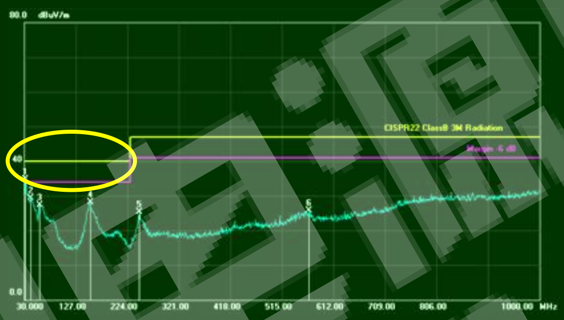




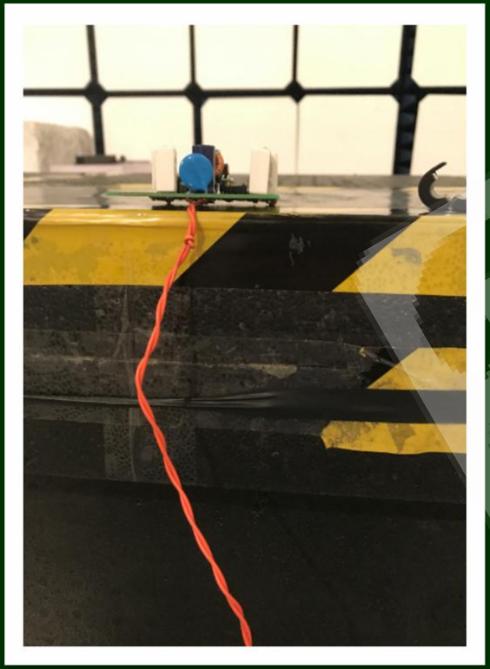
# AP0624S05LY Radiated Emission

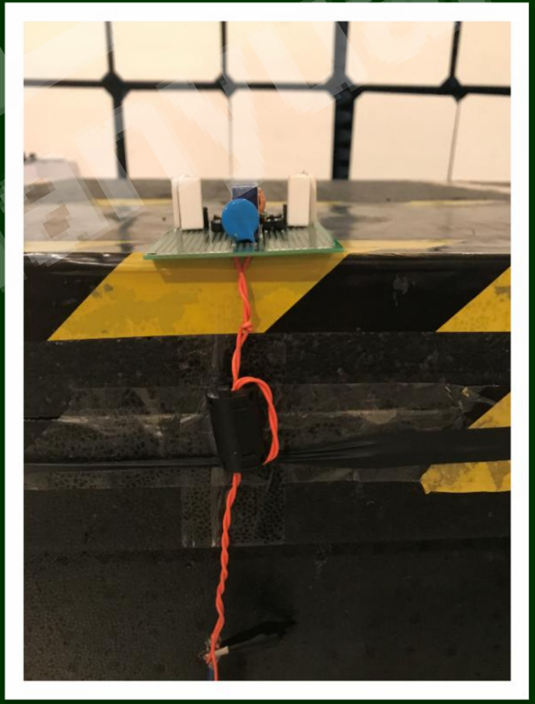


No improvement with metal case




Cable antenna radiation





# EMI Checklist

| No. | Check items |
|---|---|
| 1 | Place the component orderly according to the direction of power flow |
| 2 | Place the EMI filter as close to the input power port as possible |
| 3 | Place critical components and route critical trace first. |
| 4 | Make the loop area for high di/dt path as small as possible |
| 5 | Minimize trace area with high dV/dt |
| 6 | Place high frequency capacitors close to switching circuit |
| 7 | Minimize length of trace which is connected to Y capacitance |
| 8 | Reserve snubber at switching node |
| 9 | Reserve MOSFET gate resistor if possible |
| 10 | Heatsink shall be grounded |

# Thank you!